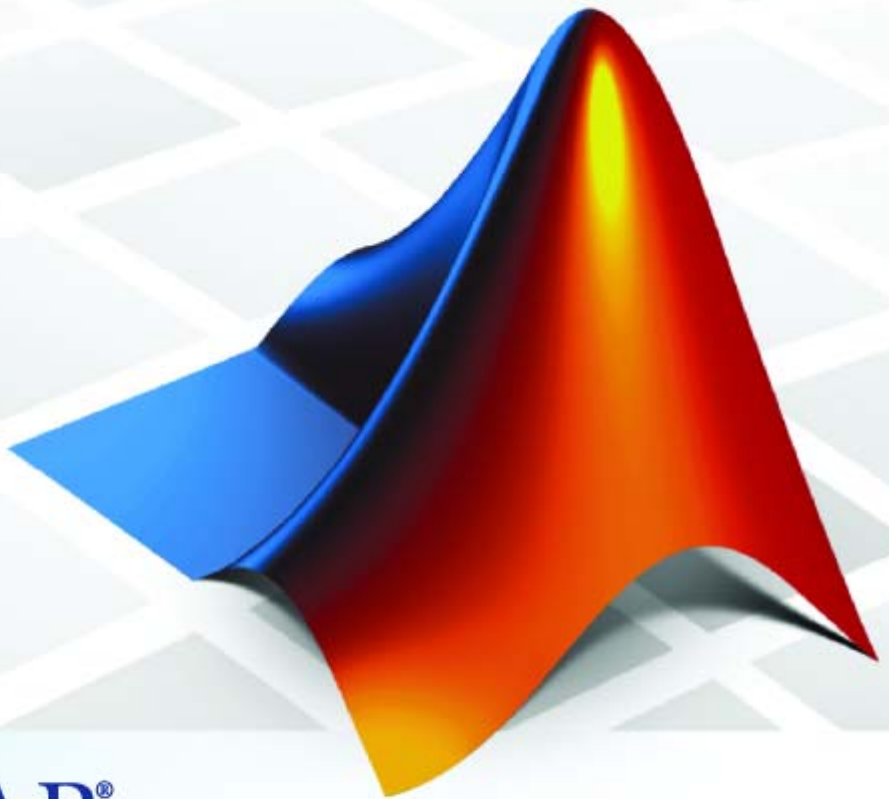


# Simulink® HDL Coder 1 User's Guide



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*Simulink HDL Coder User's Guide*

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# Getting Started

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Describes key product features and components

Expected Users and Prerequisites  
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Prerequisite knowledge expected of users of this product

Software Requirements and  
Installation (p. 1-7)

Software requirements for Simulink HDL Coder; how to install the product

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## What Is Simulink HDL Coder?

In this section...
“Overview” on page 1-2
“Simulink HDL Coder in the Hardware Development Process” on page 1-2
“Summary of Key Features” on page 1-4

### Overview

Simulink® HDL Coder lets you generate hardware description language (HDL) code based on models developed in Simulink and finite-state machines developed in Stateflow®. Simulink HDL Coder brings the Simulink Model-Based Design approach into the domain of application-specific integrated circuit (ASIC) and field programmable gate array (FPGA) development. Using Simulink HDL Coder, system architects and designers can spend more time on fine-tuning algorithms and models through rapid prototyping and experimentation and less time on HDL coding.

### Simulink HDL Coder in the Hardware Development Process

Typically, you use Simulink to model a design intended for realization as an ASIC or FPGA. Once satisfied that the model meets design requirements, you run the Simulink HDL Coder compatibility checker utility to examine model semantics and blocks for HDL code generation compatibility. You then invoke the Simulink HDL Coder code generator, using either the MATLAB® command line or the Simulink graphical user interface. Simulink HDL Coder generates VHDL or Verilog code that implements the design embodied in the model.

Usually, you also generate a corresponding test bench. You can use the test bench with HDL simulation tools such as ModelSim® to drive the generated HDL code and evaluate its behavior. Simulink HDL Coder generates scripts that automate the process of compiling and simulating your code in these tools. You can also use the MathWorks Link for ModelSim or Link for Cadence® Incisive® software to cosimulate generated HDL entities within a Simulink model.

The test bench feature increases confidence in the correctness of the generated code and saves time spent on test bench implementation. The design and test process is fully iterative. At any point, you can return to the original Simulink model, make modifications, and regenerate code.

When the design and test phase of the project has been completed, you can easily export the generated HDL code to synthesis and layout tools for hardware realization. Simulink HDL Coder generates synthesis scripts for the Synplify family of synthesis tools.

### **Extending the Code Generation Process**

Simulink HDL Coder provides a number of ways to extend the code generation process.

By attaching a *code generation control file* to your model, you can direct many details of the code generation process. At the simplest level, you can use a control file to set code generation options; such a control file could be used as a template for code generation in your organization.

Control files also let you specify how code is generated for selected sets of blocks within the model. Simulink HDL Coder provides alternate HDL *block implementations* for a variety of blocks. You can use statements in a control file to select from among implementations optimized for characteristics such as speed, chip area, or low latency.

In some cases, block-specific optimizations may introduce latencies (delays) or numeric computations (for example, saturation or rounding operations) in the generated code that are not in the original Simulink model. To help you evaluate such cases, Simulink HDL Coder creates a *generated model* — a Simulink model that corresponds exactly to the generated HDL code. This generated model lets you run simulations that produce results that are bit-true to the HDL code, and whose timing is cycle-accurate with respect to the HDL code.

You can interface Simulink HDL Coder generated HDL to existing or legacy HDL code. One way to do this is to use a subsystem in your Simulink model as a placeholder for an HDL entity, and generate a *black box* interface (comprising I/O port definitions only) to that entity. Another way is to generate a cosimulation interface by placing an HDL Cosimulation block in your model.

## Summary of Key Features

Key features and components of Simulink HDL Coder include

- Generation of synthesizable VHDL or Verilog code from Simulink models and Stateflow charts
- Code generation configured and initiated via graphical user interface, MATLAB command line interface, or M-file programs
- Test bench generation (VHDL or Verilog) for validating generated code
- Generation of models that are bit-true and cycle-accurate with respect to generated HDL code
- Numerous options for controlling the contents and style of the generated HDL code and test bench
- Block support:
  - Simulink built-in
  - Signal Processing Blockset
  - Link for ModelSim HDL Cosimulation block
  - Link for Cadence Incisive HDL Cosimulation block
  - Stateflow chart
  - Embedded MATLAB Function block
  - User-selectable optimized block implementations provided for commonly used blocks
- Code generation control files support:
  - Selection of alternate block implementations for specific blocks or sets of blocks in the model
  - Setting of code generation options
  - Selection of the model or subsystem from which code is to be generated.
  - Definition of default or template HDL code generation settings for your organization
- Generation of subsystem-based identification comments and mapping files for easy tracing of HDL entities back to corresponding elements of the original model

- Generation of interfaces to existing HDL code via:
  - Black box subsystem implementation
  - Cosimulation with ModelSim HDL simulator (requires Link for ModelSim)
  - Cosimulation with Cadence Incisive HDL simulator (requires Link for Cadence Incisive software)
- Compatibility checker utility that examines your model for HDL code generation compatibility, and generates HTML report with hyperlinks to problematic blocks
- Generation of scripts for EDA tools:
  - ModelSim
  - Synplify
- Model features supported for code generation:
  - Real data types only (fixed-point and double)  
(Complex data types are not supported.)
  - Fixed-step, discrete, single-rate and multirate models
  - Scalar and vector ports (row or column vectors only)

## **Expected Users and Prerequisites**

Simulink HDL Coder users are system and hardware architects and designers who develop, optimize, and verify ASICs or FPGAs. These designers are experienced with VHDL or Verilog but can benefit from automated HDL code generation.

Users are expected to have prerequisite knowledge in the following areas:

- Hardware design and system integration
- VHDL or Verilog
- MATLAB
- Simulink
- Simulink Fixed Point
- Signal Processing Blockset
- HDL simulators, such as ModelSim or Cadence Incisive
- Synthesis tools, such as Synplify

# Software Requirements and Installation

In this section...
“Software Requirements” on page 1-7
“Installing the Software” on page 1-8

## Software Requirements

Simulink HDL Coder requires the following products (version numbers correspond to MATLAB Release 2006b):

- MATLAB
- Simulink
- Simulink Fixed Point
- Fixed-Point Toolbox

The following related products are recommended for use with Simulink HDL Coder:

- Stateflow
- Filter Design HDL Coder

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**Note** Filter Design HDL Coder is required for generating HDL code for the Digital Filter block in certain cases. See “Summary of Block Implementations” on page 5-35.

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- [Link for ModelSim](#)
- [Link for Cadence Incisive](#)
- Signal Processing Toolbox
- Signal Processing Blockset

## **Software Requirements for Simulink HDL Coder Demos**

To operate some demos shipped with this release, the following related products are required:

- Filter Design Toolbox
- Filter Design HDL Coder
- Link for ModelSim
- Communications Toolbox (required to use Viterbi Decoder demo)
- Communications Blockset (required to use Viterbi Decoder demo)

## **VHDL and Verilog Language Support**

Before installing Simulink HDL Coder, make sure that you have compatible compilers and other tools. Simulink HDL Coder is compatible with HDL compilers, simulators and other tools that support

- VHDL versions 93 and 02
- Verilog-2001 (IEEE 1364-2001) or later

## **Installing the Software**

For information on installing the required software listed previously, and optional software, see the MATLAB installation documentation for your platform.

After completing your installation, work through the examples in Chapter 2, “Introduction to HDL Code Generation”, to acquaint yourself with the operation of the product.



## Available Help and Demos

In this section...
“Online Help” on page 1-9
“Demos” on page 1-9

### Online Help

The following online help is available:

- Online help is available in the MATLAB Help browser. Click the Simulink HDL Coder product link in the browser’s Contents pane.
- Documentation in PDF format is available through the Simulink HDL Coder roadmap page in the MATLAB Help browser. Click the **Simulink HDL Coder > Printable Documentation (PDF)** link in the browser’s Contents pane.
- M-help for the command line interface functions `makehdl`, `makehdltb`, `checkhdl`, `hdl1lib`, and `hdlsetup` is available through the MATLAB `doc` and `help` commands. For example:

```
help makehdl
```

### Demos

Simulink HDL Coder provides a number of models demonstrating aspects of HDL code generation. To access the demo models:

- 1 Type the following command at the MATLAB prompt:

```
demods
```

- 2 The **Help** window opens.
- 3 In the **Demos** pane on the left, select **Simulink > Simulink HDL Coder**.
- 4 The right pane displays hyperlinks to the available demos. Click the link to the desired demo and follow the demo instructions.



# Introduction to HDL Code Generation

---

Overview of Exercises (p. 2-2)

Overview of what you will learn in the exercises in this chapter

The `sfir_fixed` Demo Model (p. 2-3)

Description of demo model that is used in code generation exercises

Generating HDL Code Using MATLAB Commands (p. 2-6)

Generating VHDL and Verilog code and test benches in the MATLAB command line environment

Generating HDL Code in the Simulink GUI (p. 2-15)

Generating VHDL and Verilog code and test benches using the Simulink Configuration Parameters dialog box

Simulating and Verifying Generated HDL Code (p. 2-32)

Using an HDL simulator to verify generated HDL code

## Overview of Exercises

Simulink HDL Coder supports HDL code generation in your choice of environments:

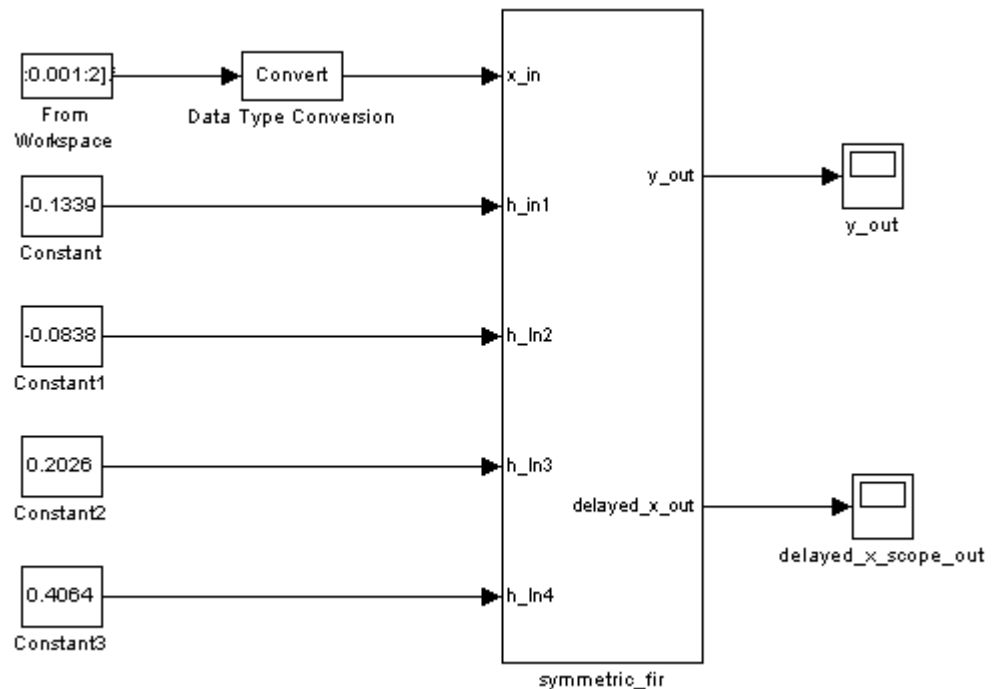
- The MATLAB Command Window supports code generation using the `makehdl`, `makehdltb`, and other functions.
- The Simulink graphical environment (the Simulink Configuration Parameters dialog box and/or Model Explorer) provides an integrated view of the model simulation parameters and HDL code generation parameters and functions.

The hands-on exercises in this chapter introduce you to the mechanics of generating and simulating HDL code with Simulink HDL Coder, using the same model to generate code in both environments. In a series of steps, you will

- Configure a simple Simulink model for code generation.
- Generate VHDL code from a subsystem of the model.
- Generate a VHDL test bench and scripts for the ModelSim HDL simulator to drive a simulation of the model.
- Compile and execute the model and test bench code in ModelSim.
- Generate and simulate Verilog code from the same model.
- Check a model for compatibility with Simulink HDL Coder.

## The sfir\_fixed Demo Model

Simulink HDL Coder provides the `sfir_fixed` demo model as a source model for HDL code generation. The model simulates a symmetric finite impulse response (FIR) filter algorithm, implemented with fixed-point arithmetic. The following figure shows the top level of the model.



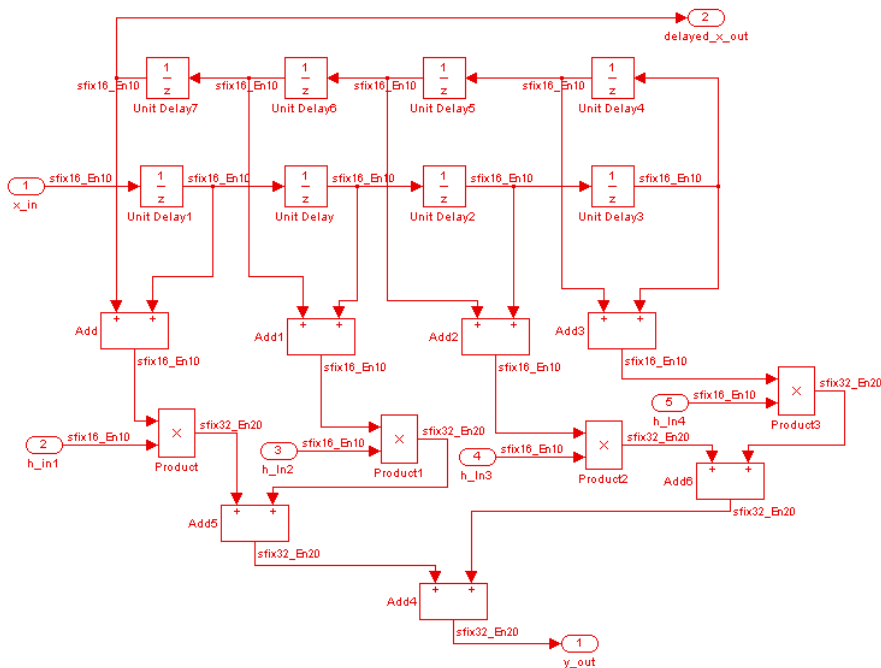
This model employs a division of labor that is useful in HDL design:

- The `symmetric_fir` subsystem, which implements the filter algorithm, is the device under test (DUT). An HDL entity will be generated, tested, and eventually synthesized from this subsystem.
- The top-level model components that drive the subsystem work as a test bench.

The top-level model generates 16-bit fixed-point input signals for the `symmetric_fir` subsystem. The Signal From Workspace block generates a test input (stimulus) signal for the filter. The four Constant blocks provide filter coefficients.

The Scope blocks are used in Simulink simulation only. They are virtual blocks, and do not generate any HDL code.

The following figure shows the `symmetric_fir` subsystem.



Simulink propagates appropriate fixed-point data types throughout the subsystem. Inputs inherit the data types of the signals presented to them. Where required, internal rules of the blocks determine the correct output data type, given the input data types and the operation performed (for example, the Product blocks output 32-bit signals).

The filter outputs a 32-bit fixed-point result at the `y_out` port, and also replicates its input (after passing it through several delay stages) at the `delayed_x_out` port.

In the exercises that follow, you generate VHDL code that implements the `symmetric_fir` subsystem as an entity. You then generate a test bench from the top-level model. The test bench drives the generated entity, for the required number of clock steps, with stimulus data generated from the Signal From Workspace block.

## Generating HDL Code Using MATLAB Commands

In this section...
“Overview” on page 2-6
“Creating a Directory and Local Model File” on page 2-6
“Initializing Model Parameters with hdlsetup” on page 2-7
“Generating a VHDL Entity from a Subsystem” on page 2-9
“Generating VHDL Test Bench Code” on page 2-11
“Verifying Generated Code” on page 2-12
“Generating a Verilog Module and Test Bench” on page 2-13

### Overview

This exercise provides a step-by-step introduction to the Simulink HDL Coder code and test bench generation commands, their arguments, and the files created by the code generator. The exercise assumes that you have familiarized yourself with the demo model (see “The sfir\_fixed Demo Model” on page 2-3).

### Creating a Directory and Local Model File

Make a local copy of the demo model and store it in a working directory, as follows.

**1** Start MATLAB.

**2** Create a directory named `sl_hdlcoder_work`, for example:

```
mkdir C:\work\sl_hdlcoder_work
```

The `sl_hdlcoder_work` directory will store a local copy of the demo model and to store directories and code generated by Simulink HDL Coder. The location of the directory does not matter, except that it should not be within the MATLAB directory tree.

**3** Make the `sl_hdlcoder_work` directory your working directory, for example:



```
cd C:\work\sl_hdlcoder_work
```

- 4 To open the demo model, type the following command at the MATLAB prompt:

```
demods
```

- 5 The **Help** window opens. In the **Demos** pane on the left, click the + for **Simulink**. Then click the + for **Simulink HDL Coder**. Then double-click the list entry for the Symmetric FIR Filter Demo.

The `sfir_fixed` model opens.

- 6 Select **Save As** from the Simulink **File** menu and save a local copy of `sfir_fixed.mdl` to your working directory.
- 7 Leave the `sfir_fixed` model open and proceed to the next section.

## Initializing Model Parameters with `hdlsetup`

Before generating code, you must set some parameters of the model. Rather than doing this manually, use the Simulink HDL Coder M-file utility, `hdlsetup.m`. The `hdlsetup` command uses the Simulink `set_param` function to set up models for HDL code generation quickly and consistently.

To set the model parameters:

- 1 At the MATLAB command prompt, type

```
hdlsetup('sfir_fixed')
```

- 2 Select **Save** from the Simulink **File** menu, to save the model with its new settings.

Before continuing with code generation, consider the settings that `hdlsetup` applies to the model.

`hdlsetup` configures Simulink **Solver** options that are recommended or required by Simulink HDL Coder. These are

- **Type:** Fixed-step. Simulink HDL Coder does not currently support variable-step solvers.
- **Solver:** discrete (no continuous states). Other fixed-step solvers could be selected, but this option is usually the correct one for simulating discrete systems.
- **Tasking mode:** SingleTasking. Simulink HDL Coder does not currently support models that execute in multitasking mode.

Do not set **Tasking mode** to Auto.

hdlsetup also configures the model start and stop times and fixed-step size as follows:

- **Start Time:** 0.0 s
- **Stop Time:** 10 s
- **Fixed step size (fundamental periodic sample time):** auto

Setting **Fixed step size** to auto causes Simulink to choose the step size, based on the sample times specified in the model. In the demo model, only the Signal From Workspace block specifies an explicit sample time (1 s); all other blocks inherit this sample time.

The model start and stop times determine the total simulation time. This in turn determines the size of data arrays that are generated to provide stimulus and output data for generated test benches. For the demo model, computation of 10 seconds of test data does not take a significant amount of time. Computation of sample values for more complex models can be time consuming. In such cases, you may want to decrease the total simulation time.

The remaining parameters set by hdlsetup affect Simulink error severity levels, data logging, and model display options. If you want to view the complete set of model parameters affected by hdlsetup, open hdlsetup.m in the MATLAB editor.

The model parameter settings provided by hdlsetup are intended as useful defaults, but they may not be appropriate for all your applications. For example, hdlsetup sets a default **Simulation stop time** of 10 s. A total simulation time of 1000 s would be more realistic for a test of the sfir\_fixed

demo model. If you would like to change the simulation time, enter the desired value into the **Simulation stop time** field of the Simulink window.

See the “Model Parameters” table in the “Model and Block Parameters” section of the Simulink documentation for a summary of user-settable model parameters.

## Generating a VHDL Entity from a Subsystem

In this section, you will use the `makehdl` function to generate code for a VHDL entity from the `symmetric_fir` subsystem of the demo model. `makehdl` also generates script files for third-party HDL simulation and synthesis tools.

`makehdl` lets you specify numerous properties that control various features of the generated code. In this example, you will use defaults for all `makehdl` properties.

Before generating code, make sure that you have completed the steps described in “Creating a Directory and Local Model File” on page 2-6 and “Initializing Model Parameters with `hdlsetup`” on page 2-7.

To generate code:

- 1 Select **Current Directory** from the **Desktop** menu in the MATLAB window. This displays the MATLAB Current Directory browser, which lets you easily access your working directory and the files that will be generated within it.
- 2 At the MATLAB prompt, type the command

```
makehdl('sfir_fixed/symmetric_fir')
```

This command directs Simulink HDL Coder to generate code from the `symmetric_fir` subsystem within the `sfir_fixed` model, using default values for all properties.

- 3 Simulink HDL Coder generates code and displays progress messages. The process should complete successfully with the message

```
### HDL Code Generation Complete.
```

Observe that the names of generated files in the progress messages are hyperlinked. After code generation completes, you can click these hyperlinks to view the files in the MATLAB editor.

makehdl compiles the model before generating code. Depending on model display options (for example, sample time colors, port data types, etc.), the appearance of the model may change after code generation.

- 4** By default, makehdl generates VHDL code. Code files and scripts are written to a *target directory*. The default target directory is a subdirectory of your working directory, named hdlsrc.

A folder icon for the hdlsrc directory is now visible in the Current Directory browser. To view generated code and script files, double-click the hdlsrc folder icon.

- 5** The files that makehdl has generated in the hdlsrc directory are
  - `symmetric_fir.vhd`: VHDL code. This file contains an entity definition and RTL architecture implementing the `symmetric_fir` filter.
  - `symmetric_fir_compile.do`: ModelSim compilation script (`vcom` command) to compile the generated VHDL code.
  - `symmetric_fir_synplify.tcl`: Synplify synthesis script
  - `symmetric_fir_map.txt`: Mapping file. This report file maps generated entities (or modules) to the Simulink subsystems that generated them (see “Code Tracing Using the Mapping File” on page 7-6).
- 6** To view the generated VHDL code in the MATLAB editor, double-click the `symmetric_fir.vhd` file icon in the Current Directory browser.

At this point it is suggested that you study the ENTITY and ARCHITECTURE definitions while referring to “HDL Code Generation Defaults” on page 14-15 in the makehdl reference documentation. The reference documentation describes the default naming conventions and correspondences between the elements of a Simulink model (subsystems, ports, signals, etc.) and elements of generated HDL code.

- 7** Before proceeding to the next section, close any files you have opened in the MATLAB editor. Then, click the Go Up One Level button in the

Current Directory browser, to set the current directory back to your `sl_hdlcoder_work` directory.

**8** Leave the `sfir_fixed` model open and proceed to the next section.

## Generating VHDL Test Bench Code

In this section, you use the Simulink HDL Coder test bench generation function, `makehdltb`, to generate a VHDL test bench. The test bench is designed to drive and verify the operation of the `symmetric_fir` entity that was generated in the previous section. A generated test bench includes

- Stimulus data generated by signal sources connected to the entity under test.
- Output data generated by the entity under test. During a test bench run, this data is compared to the outputs of the VHDL model, for verification purposes.
- Clock, reset, and clock enable inputs to drive the entity under test.
- A component instantiation of the entity under test.
- Code to drive the entity under test and compare its outputs to the expected data.

In addition, `makehdltb` generates ModelSim scripts to compile and execute the test bench.

This exercise assumes that your working directory is the same as that used in the previous section. This directory now contains an `hdlsrc` folder containing the previously generated code.

To generate a test bench:

**1** At the MATLAB prompt, type the command

```
makehdltb('sfir_fixed/symmetric_fir')
```

This command generates a test bench that is designed to interface to and validate code generated from `symmetric_fir` (or from a subsystem with a functionally identical interface). By default, VHDL test bench code, as well as scripts, are generated in the `hdlsrc` target directory.

- 2 Simulink HDL Coder generates code and displays progress messages. The process should complete successfully with the message

```
### HDL TestBench Generation Complete.
```

- 3 To view generated test bench and script files, double-click the `hdlsrc` folder icon in the Current Directory browser. Alternatively, you can click the hyperlinked names of generated files in the code test bench generation progress messages.

The files generated by `makehdltb` are

- `symmetric_fir_tb.vhd`: VHDL test bench code and generated test and output data.
  - `symmetric_fir_tb_compile.do`: ModelSim compilation script (`vcom` commands). This script compiles and loads both the entity to be tested (`symmetric_fir.vhd`) and the test bench code (`symmetric_fir_tb.vhd`).
  - `symmetric_fir_tb_sim.do`: ModelSim script to initialize the simulator, set up **wave** window signal displays, and run a simulation.
- 4 If you want to view the generated test bench code in the MATLAB editor, double-click the `symmetric_fir.vhd` file icon in the Current Directory browser. You may want to study the code while referring to the `makehdltb` reference documentation, which describes the default actions of the test bench generator.
  - 5 Before proceeding to the next section, close any files you have opened in the MATLAB editor. Then, click the Go Up One Level button in the Current Directory browser, to set the current directory back to your `sl_hdlcoder_work` directory.

## Verifying Generated Code

You can now take the previously generated code and test bench to an HDL simulator for simulated execution and verification of results. See “Simulating and Verifying Generated HDL Code” on page 2-32 for an example of how to use generated test bench and script files with the Mentor Graphics HDL simulator, ModelSim SE/PE.

## Generating a Verilog Module and Test Bench

The procedures for generating Verilog code differ only slightly from those for generating VHDL code. This section provides an overview of the command syntax and the generated files.

### Generating a Verilog Module

By default, `makehdl` generates VHDL code. To override the default and generate Verilog code, you must pass in a property/value pair to `makehdl`, setting the `TargetLanguage` property to `'verilog'`, as in this example.

```
makehdl('sfir_fixed/symmetric_fir','TargetLanguage','verilog')
```

The previous command generates Verilog source code, as well as ModelSim and Synplify scripts, in the default target directory, `hdlsrc`.

The files generated by this example command are

- `symmetric_fir.v`: Verilog code. This file contains a Verilog module implementing the `symmetric_fir` subsystem.
- `symmetric_fir_compile.do`: ModelSim compilation script (`vlog` command) to compile the generated Verilog code.
- `symmetric_fir_synplify.tcl`: Synplify synthesis script.
- `symmetric_fir_map.txt`: Mapping file. This report file maps generated entities (or modules) to the Simulink subsystems that generated them (see “Code Tracing Using the Mapping File” on page 7-6).

### Generating and Executing a Verilog Test Bench

The `makehdltb` syntax for overriding the target language is exactly the same as that for `makehdl`. The following example generates Verilog test bench code to drive the Verilog module, `symmetric_fir`, in the default target directory.

```
makehdltb('sfir_fixed/symmetric_fir','TargetLanguage','verilog')
```

The files generated by this example command are

- `symmetric_fir_tb.v`: Verilog test bench code and generated test and output data.
- `symmetric_fir_tb_compile.do`: ModelSim compilation script (vlog commands). This script compiles and loads both the entity to be tested (`symmetric_fir.v`) and the test bench code (`symmetric_fir_tb.v`).
- `symmetric_fir_tb_sim.do`: ModelSim script to initialize the simulator, set up **wave** window signal displays, and run a simulation.

The following listing shows the commands and responses from a ModelSim test bench session using the generated scripts.

```
ModelSim>vlib work
ModelSim> do symmetric_fir_tb_compile.do
# Model Technology ModelSim SE vlog 6.0 Compiler 2004.08 Aug 19 2004
# -- Compiling module symmetric_fir
#
# Top level modules:
# symmetric_fir
# Model Technology ModelSim SE vlog 6.0 Compiler 2004.08 Aug 19 2004
# -- Compiling module symmetric_fir_tb
#
# Top level modules:
# symmetric_fir_tb
ModelSim>do symmetric_fir_tb_sim.do
# vsim work.symmetric_fir_tb
# Loading work.symmetric_fir_tb
# Loading work.symmetric_fir
# **** Test Complete. ****
# Break at
C:/work/sl_hdlcoder_work/vlog_code/symmetric_fir_tb.v line 142
# Simulation Breakpoint:Break at
C:/work/sl_hdlcoder_work/vlog_code/symmetric_fir_tb.v line 142
# MACRO ./symmetric_fir_tb_sim.do PAUSED at line 14
```



## Generating HDL Code in the Simulink GUI

### In this section...

“Simulink HDL Coder GUI Overview” on page 2-15

“Creating a Directory and Local Model File” on page 2-18

“Viewing Simulink HDL Coder Options in the Configuration Parameters Dialog Box” on page 2-19

“Creating a Control File” on page 2-21

“Initializing Model Parameters With hdlsetup” on page 2-24

“Selecting and Checking a Subsystem for HDL Compatibility” on page 2-26

“Generating VHDL Code” on page 2-27

“Generating VHDL Test Bench Code” on page 2-29

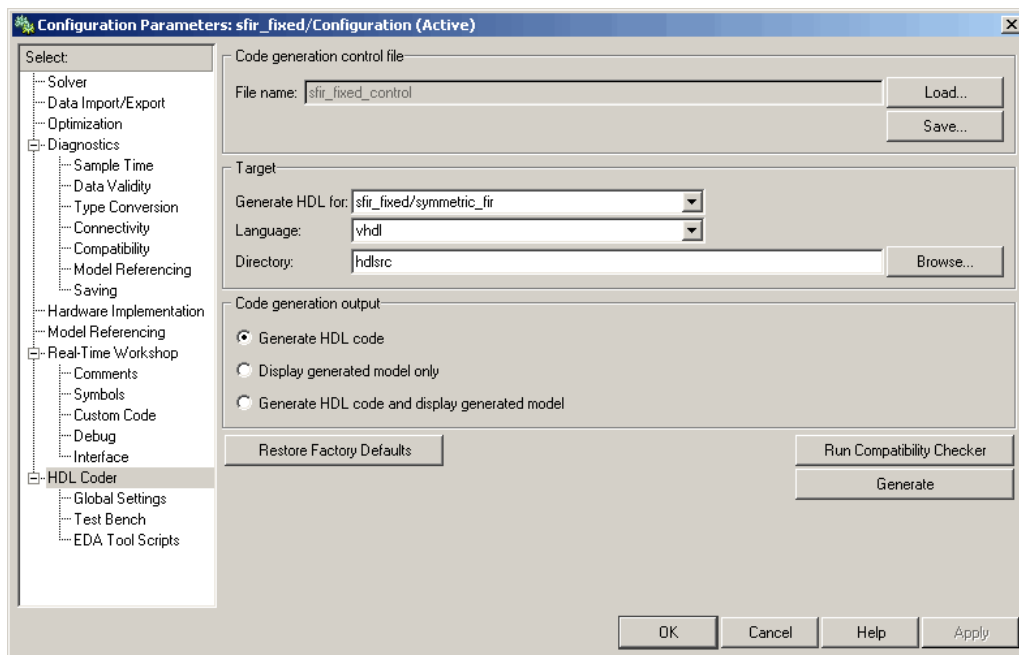
“Verifying Generated Code” on page 2-31

“Generating Verilog Model and Test Bench Code” on page 2-31

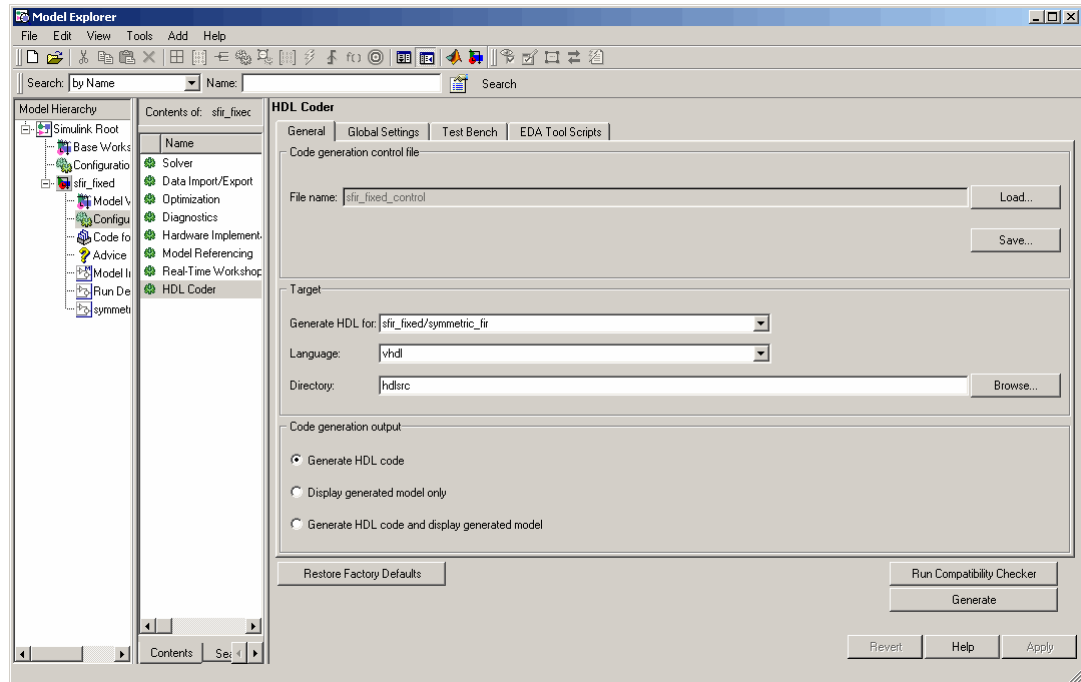
### Simulink HDL Coder GUI Overview

Simulink provides visual access to options and parameters that affect HDL code generation, within the framework of a Simulink configuration set. You can view and edit these options in the Simulink Configuration Parameters dialog box, or in the Simulink Model Explorer.

The following figure shows the top-level **HDL Coder** options pane as displayed in the Configuration Parameters dialog box.



The following figure shows the top-level **HDL Coder** options pane as displayed in the Model Explorer.



If you are not familiar with Simulink configuration sets and how to view and edit them in the Configuration Parameters dialog box, see the following sections of the Simulink documentation:

- “Configuration Sets”
- “Configuration Parameters Dialog Box”

If you are not familiar with the Model Explorer, see “Exploring, Searching, and Browsing Models” in the Simulink documentation.

In the hands-on code generation exercises that follow, you will use the Configuration Parameters dialog box view of Simulink HDL Coder options and controls. The exercises use the `sfir_fixed` demo model (see “The `sfir_fixed` Demo Model” on page 2-3) in basic code generation and verification steps.

### Creating a Directory and Local Model File

In this section you will setup the directory and a local copy of the demo model.

#### Creating a Directory

Start by setting up a working directory:

- 1 Start MATLAB.
- 2 Create a directory named `sl_hdlcoder_work`, for example:

```
mkdir C:\work\sl_hdlcoder_work
```

You will use `sl_hdlcoder_work` to store a local copy of the demo model and to store directories and code generated by Simulink HDL Coder. The location of the directory does not matter, except that it should not be within the MATLAB directory tree.

- 3 Make the `sl_hdlcoder_work` directory your working directory, for example:

```
cd C:\work\sl_hdlcoder_work
```

#### Making a Local Copy of the Model File

Next, make a copy of the `sfir_fixed` demo model:

- 1 To open the demo model, type the following command at the MATLAB prompt:

```
demons
```

The **Help** window opens.

- 2 In the **Demos** pane on the left, click the + for **Simulink**. Then click the + for **Simulink HDL Coder**. Then double-click the list entry for the Symmetric FIR Filter Demo.

The `sfir_fixed` model opens.

- 3 Select **Save As** from the Simulink **File** menu and save a local copy of `sfir_fixed.mdl` to your working directory.
- 4 Leave the `sfir_fixed` model open and proceed to the next section.

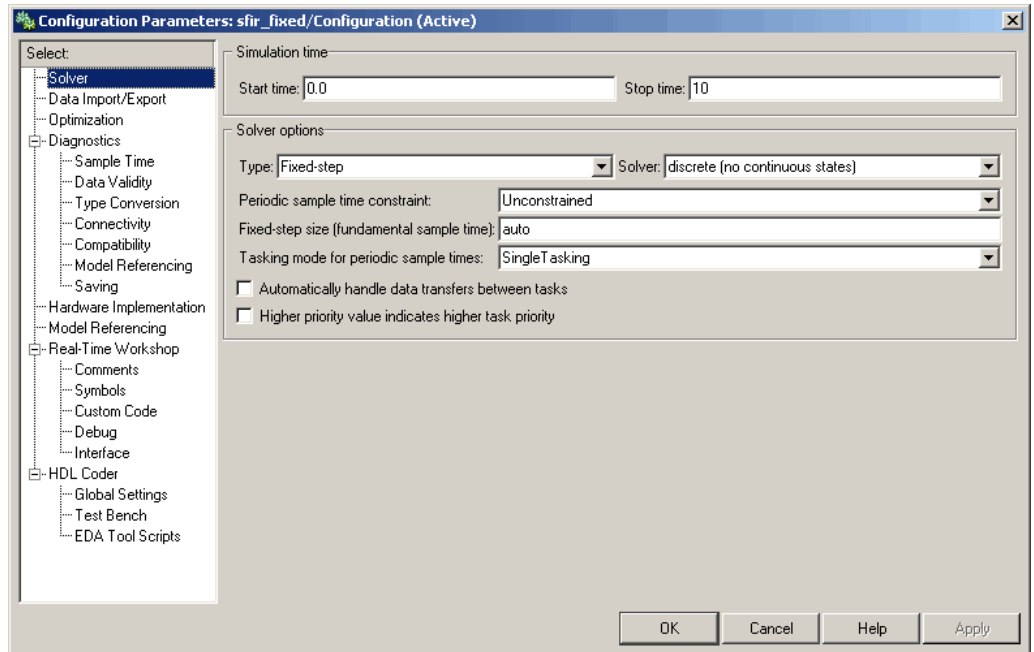
## Viewing Simulink HDL Coder Options in the Configuration Parameters Dialog Box

The Simulink HDL Coder option settings are displayed as a category of the model's active configuration set. You can view and edit these options in the Configuration Parameters dialog box, or in the Simulink Model Explorer. This discussion uses the Configuration Parameters dialog box.

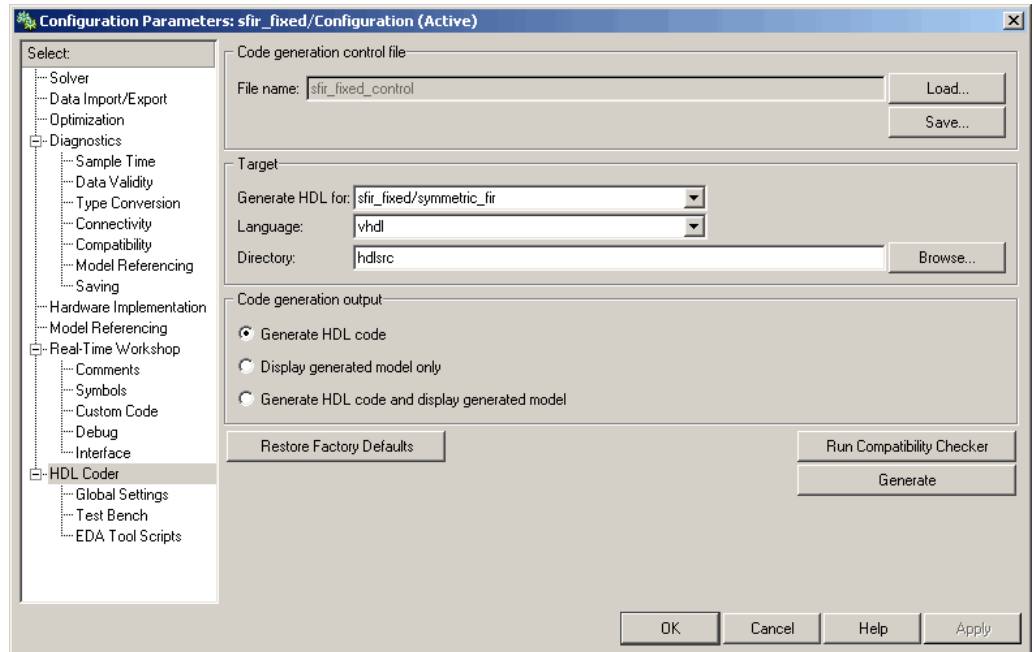
To access the Simulink HDL Coder settings:

- 1 Select **Configuration Parameters** from the **Simulation** menu in the `sfir_fixed` model window.

The Configuration Parameters dialog box opens with the **Solver** options pane displayed, as shown in the following figure.



- 2 Observe that the **Select** tree in the left panel of the dialog box includes an **HDL Coder** category, as shown.
- 3 Click the **HDL Coder** category in the **Select** tree. The **HDL Coder** pane is displayed, as shown in the following figure.



The **HDL Coder** pane contains top-level options and buttons that control the HDL code generation process. Several other categories of options are available under the **HDL Coder** entry in the **Select** tree. This exercise uses a small subset of these options, leaving the others at their default settings.

Chapter 3, “Code Generation Options in the Simulink HDL Coder GUI” summarizes all the options available in the **HDL Coder** category.

## Creating a Control File

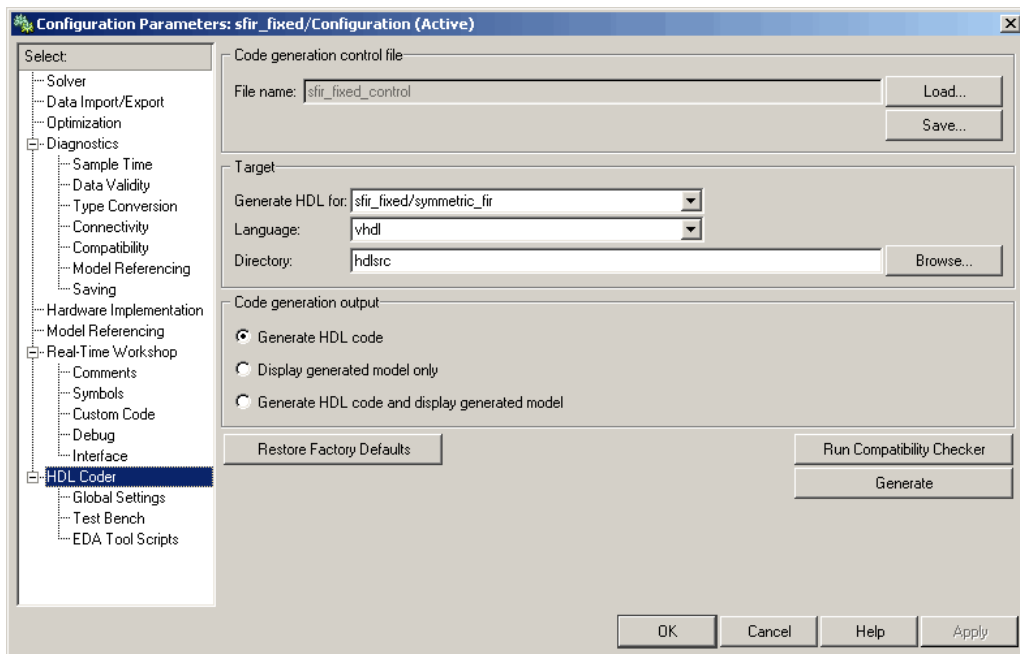
Simulink HDL Coder *code generation control files* (referred to in this document as *control files*) let you

- Save your model’s Simulink HDL Coder options.
- Extend the HDL code generation process and direct its details.

A control file is an M-file that you attach to your model, using either the `makehdl` command or the Simulink Configuration Parameters dialog box. In

this tutorial, you will use a control file to save Simulink HDL Coder options. This is a required step with most models, because Simulink HDL Coder settings are not saved in the .mdl file like other components of a model's configuration set. If you want your Simulink HDL Coder settings to persist across sessions with a model, you must save your current Simulink HDL Coder settings to a control file. The control file is then linked to the model, and the linkage is preserved when you save the model.

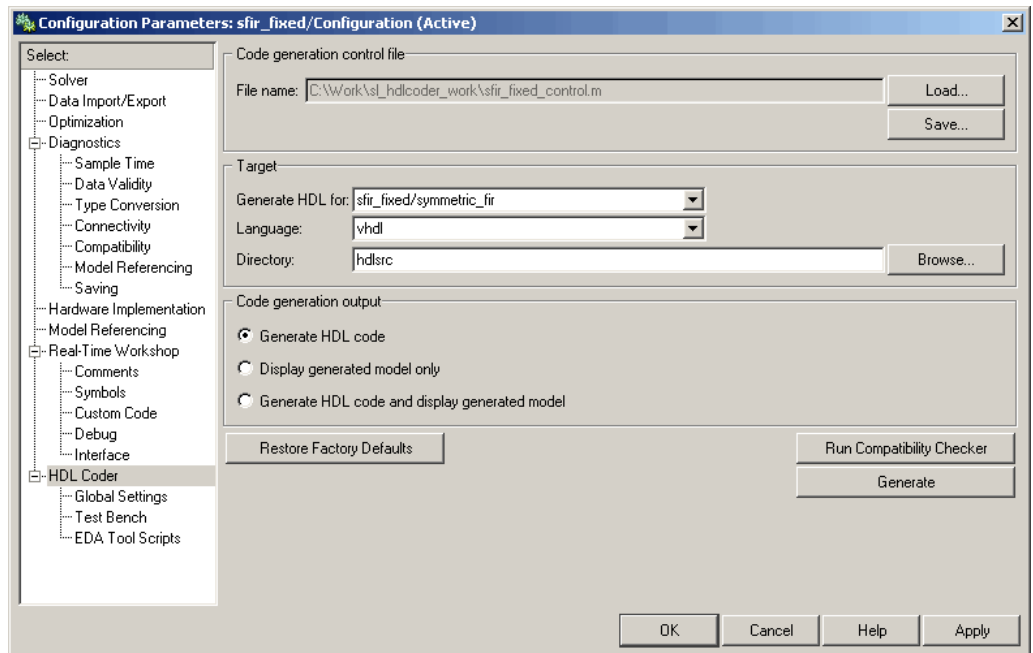
When a control file is linked to a model, the control file name is displayed in the **File name** field of the top-level **HDL Coder** options pane. The `sfir_fixed` demo model is attached to the control file `sfir_fixed_control.m`. This control file is stored within the MATLAB demo directories and should not be overwritten. For use in this tutorial, you will save the current Simulink HDL Coder options to a new control file in the working directory. Later in the tutorial, you will change some Simulink HDL Coder options and save them to the control file.



To save the current Simulink HDL Coder options to a new control file:



- 1 Open the Configuration Parameters dialog box and select the **HDL Coder** options pane.
- 2 Under **Code generation control file**, click the **Save** button. A standard file dialog box opens.
- 3 Navigate to your current working directory and save the file as `sfir_fixed_control.m`.
- 4 The **File name** field updates to show the linkage to the new control file name (with full absolute path and extension), as shown in the following figure.



- 5 Click **Apply**.
- 6 Select **Save** from the Simulink **File** menu. When you save the model, the control file linkage information is written to the `.mdl` file, and the control file linkage persists in future MATLAB sessions with your model.

This tutorial uses a control file only as a mechanism for saving Simulink HDL Coder settings. This simple application of a control file does not require knowledge of any internal details about the file. You can also use a control file to direct or customize many details of the code generation process. It is strongly recommended that you read Chapter 5, “Code Generation Control Files” after completing this tutorial.

## Initializing Model Parameters With `hdlsetup`

Before generating code, you must set some parameters of the Simulink model. Rather than doing this manually, use the Simulink HDL Coder M-file utility, `hdlsetup.m`. The `hdlsetup` command uses the Simulink `set_param` function to set up models for HDL code generation quickly and consistently.

To set the model parameters:

- 1 At the MATLAB command prompt, type

```
hdlsetup('sfir_fixed')
```

- 2 Select **Save** from the Simulink **File** menu, to save the model with its new settings.

You do not need to update the control file at this point, because `hdlsetup` modifies only the Simulink model parameters, not the HDL code generation options.

Before continuing with code generation, consider the settings that `hdlsetup` applies to the model.

`hdlsetup` configures Simulink **Solver** options that are recommended or required by Simulink HDL Coder. These are

- **Type:** Fixed-step. Simulink HDL Coder does not currently support variable-step solvers.
- **Solver:** discrete (no continuous states). Other fixed-step solvers could be selected, but this option is usually the correct one for simulating discrete systems.

- **Tasking mode:** `SingleTasking`. Simulink HDL Coder does not currently support models that execute in multitasking mode.

Do not set **Tasking mode** to `Auto`.

`hdlsetup` also configures the model start and stop times and fixed-step size as follows:

- **Start Time:** `0.0 s`
- **Stop Time:** `10 s`
- **Fixed step size (fundamental periodic sample time):** `auto`

Setting **Fixed step size** to `auto` causes Simulink to choose the step size, based on the sample times specified in the model. In the demo model, only the Signal From Workspace block specifies an explicit sample time (`1 s`); all other blocks inherit this sample time.

The model start and stop times determine the total simulation time. This in turn determines the size of data arrays that are generated to provide stimulus and output data for generated test benches. For the demo model, computation of 10 seconds of test data does not take a significant amount of time. Computation of sample values for more complex models can be time consuming. In such cases, you may want to decrease the total simulation time.

The remaining parameters set by `hdlsetup` affect Simulink error severity levels, data logging, and model display options. If you want to view the complete set of model parameters affected by `hdlsetup`, open `hdlsetup.m` in the MATLAB editor.

The model parameter settings provided by `hdlsetup` are intended as useful defaults, but they may not be appropriate for all your applications. For example, `hdlsetup` sets a default **Simulation stop time** of `10 s`. A total simulation time of `1000 s` would be more realistic for a test of the `sfir_fixed` demo model. If you would like to change the simulation time, enter the desired value into the **Simulation stop time** field of the Simulink window.

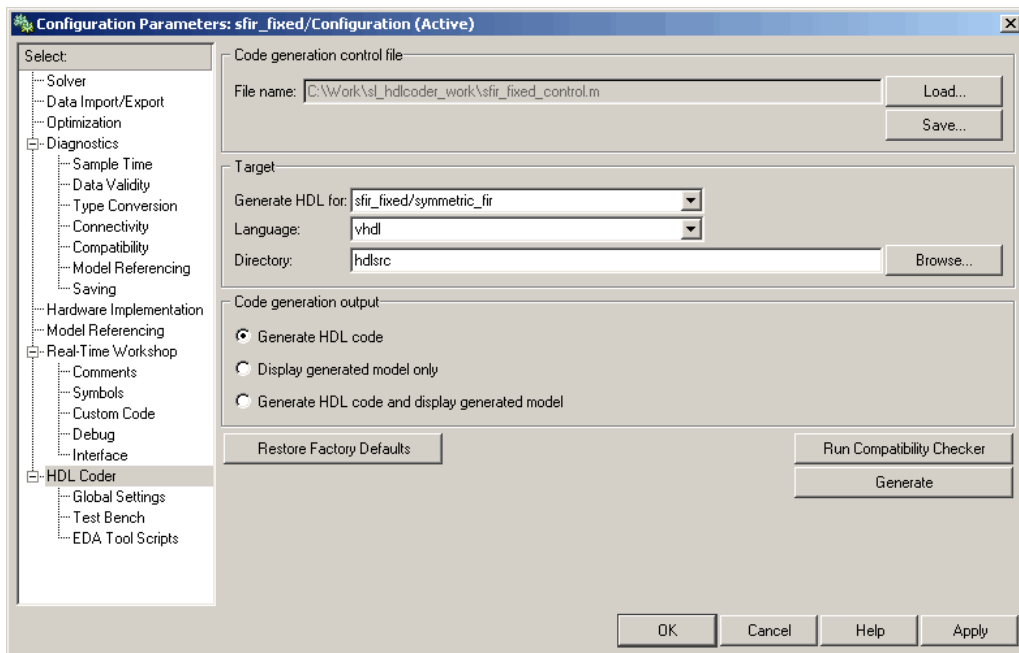
See the “Model Parameters” table in the “Model and Block Parameters” section of the Simulink documentation for a summary of user-settable model parameters.

## Selecting and Checking a Subsystem for HDL Compatibility

Simulink HDL Coder generates code from either the current model or from a subsystem at the root level of the current model. You use the **Generate HDL for** menu to select the model or subsystem from which code is to be generated. Each entry in the menu shows the full Simulink path to the model or one of its subcomponents.

The `sfir_fixed` demo model is configured with the `sfixed_fir/symmetric_fir` subsystem selected for code generation. If this is not the case, make sure that the `symmetric_fir` subsystem is selected for code generation, as follows:

- 1 Select `sfixed_fir/symmetric_fir` from the **Generate HDL for** menu.
- 2 Click **Apply**. The dialog box should now appear as shown in the following figure.

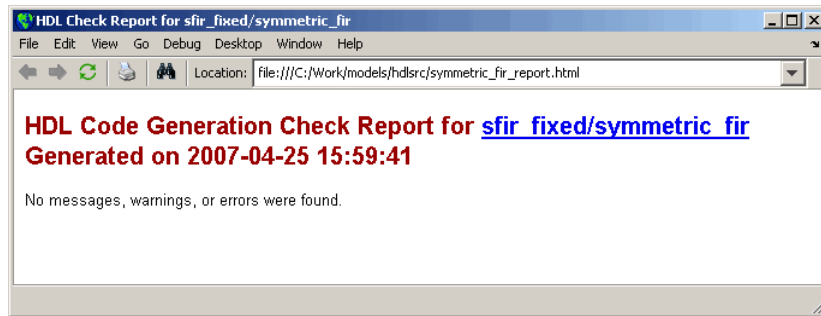


To check HDL compatibility for the subsystem:

- 1 Click the **Run Compatibility Checker** button.
- 2 The HDL compatibility checker examines the system selected in the **Generate HDL for** menu for any compatibility problems. In this case, the selected subsystem is fully HDL-compatible, and the compatibility checker displays the following message in the MATLAB Command Window.

```
### Starting HDL Check.
### HDL Check Complete with 0 errors, warnings and messages.
```

- 3 The compatibility checker also displays an HTML report in a Web browser, as shown in the following figure.

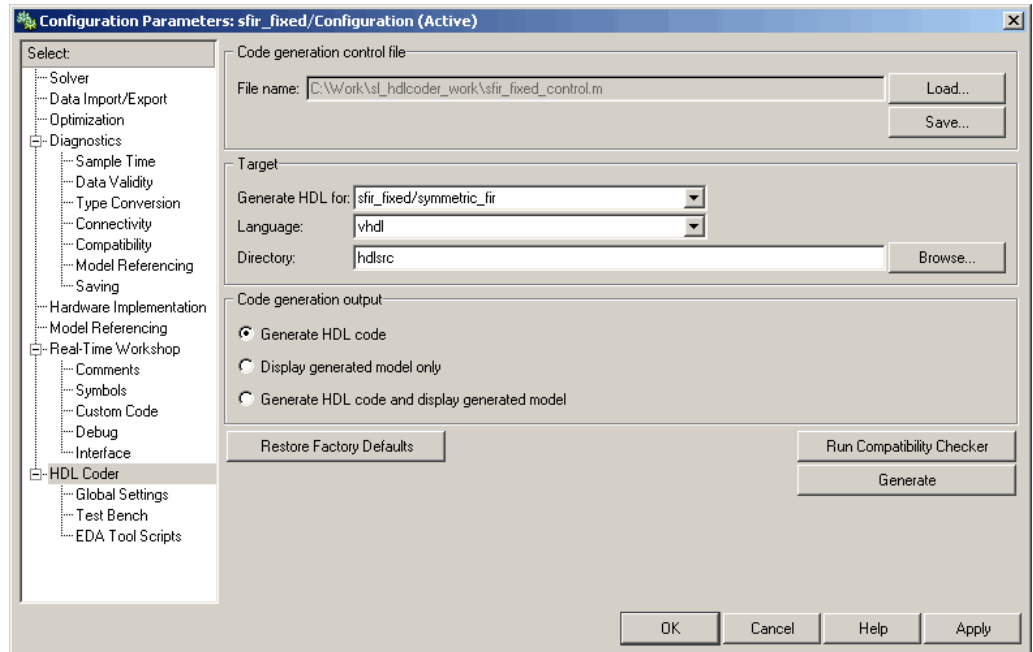


## Generating VHDL Code

The top-level **HDL Coder** options are now set as follows:

- The **Generate HDL for** field specifies the `sfixed_fir/symmetric_fir` subsystem for code generation.
- The **Language** field specifies (by default) generation of VHDL code.
- The **Directory** field specifies a *target directory* that stores generated code files and scripts. The default target directory is a subdirectory of your working directory, named `hdlsrc`.

The following figure shows these settings.



Before generating code, select **Current Directory** from the **Desktop** menu in the MATLAB window. This displays the MATLAB Current Directory browser, which lets you easily access your working directory and the files that will be generated within it.

To generate code:

- 1 Click the **Generate** button.
- 2 Simulink HDL Coder generates code and displays progress messages. The process should complete successfully with the message

```
### HDL Code Generation Complete.
```

Observe that the names of generated files in the progress messages are hyperlinked. After code generation completes, you can click these hyperlinks to view the files in the MATLAB editor.

Simulink HDL Coder compiles the model before generating code. Depending on model display options (for example, sample time colors, port data types, etc.), the appearance of the model may change after code generation.

- 3** A folder icon for the `hdlsrc` directory is now visible in the Current Directory browser. To view generated code and script files, double-click the `hdlsrc` folder icon.
- 4** The files that were generated in the `hdlsrc` directory are
  - `symmetric_fir.vhd`: VHDL code. This file contains an entity definition and RTL architecture implementing the `symmetric_fir` filter.
  - `symmetric_fir_compile.do`: ModelSim compilation script (`vcom` command) to compile the generated VHDL code.
  - `symmetric_fir_synplify.tcl`: Synplify synthesis script.
  - `symmetric_fir_map.txt`: Mapping file. This report file maps generated entities (or modules) to the Simulink subsystems that generated them (see “Code Tracing Using the Mapping File” on page 7-6).
- 5** To view the generated VHDL code in the MATLAB editor, double-click the `symmetric_fir.vhd` file icon in the Current Directory browser.

At this point it is suggested that you study the ENTITY and ARCHITECTURE definitions while referring to “HDL Code Generation Defaults” on page 14-15 in the `makehdl` reference documentation. The reference documentation describes the default naming conventions and correspondences between the elements of a Simulink model (subsystems, ports, signals, etc.) and elements of generated HDL code.

- 6** Before proceeding to the next section, close any files you have opened in the MATLAB editor. Then, click the Go Up One Level button in the Current Directory browser, to set the current directory back to your `sl_hdlcoder_work` directory.

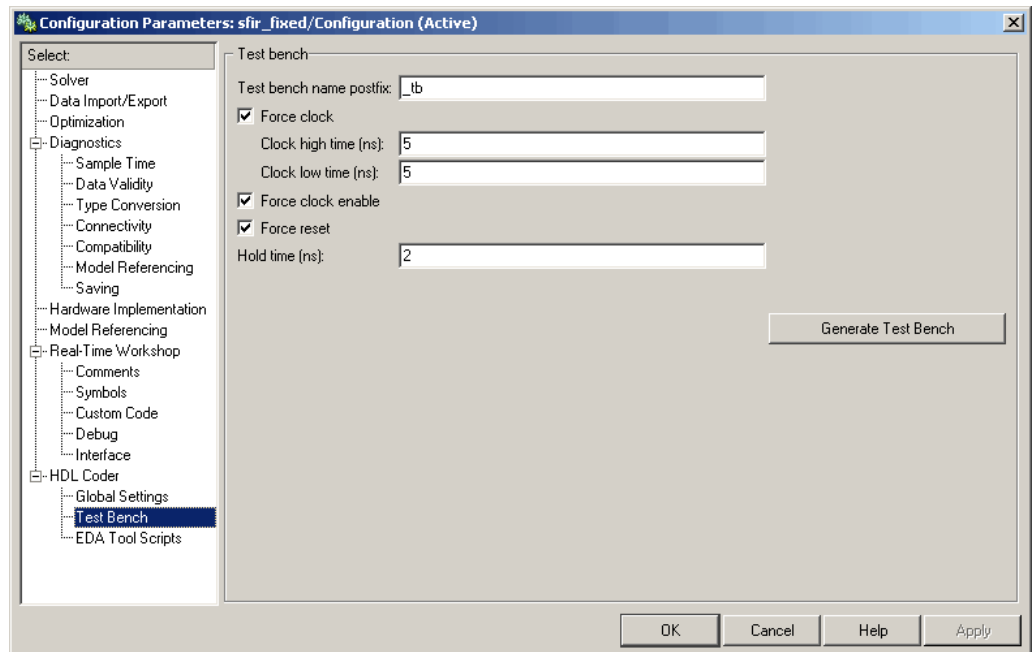
## Generating VHDL Test Bench Code

At this point, the **Generate HDL for**, **Language**, and **Directory** fields are set as they were in the previous section. Accordingly, you can now generate VHDL test bench code to drive the VHDL code generated previously for the

sfixed\_fir/symmetric\_fir subsystem. The code will be written to the same target directory as before.

To generate a test bench:

- 1 Click the **Test Bench** entry in the **HDL Coder** list in the **Select** tree. The **Test Bench** pane is displayed, as shown in the following figure.



- 2 Click the **Generate Test bench** button.
- 3 Simulink HDL Coder generates code and displays progress messages in the MATLAB window. The process should complete successfully with the message

```
### HDL TestBench Generation Complete.
```

- 4 The files that were generated in the hdlsrc directory are



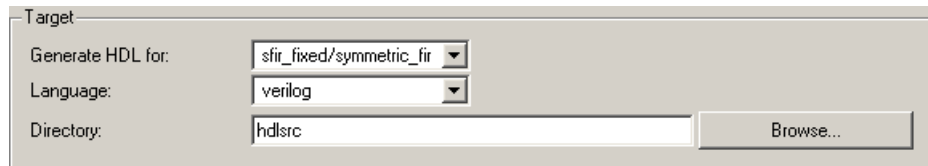
- `symmetric_fir_tb.vhd`: VHDL test bench code and generated test and output data.
- `symmetric_fir_tb_compile.do`: ModelSim compilation script (vcom commands). This script compiles and loads both the entity to be tested (`symmetric_fir.vhd`) and the test bench code (`symmetric_fir_tb.vhd`).
- `symmetric_fir_tb_sim.do`: ModelSim script to initialize the simulator, set up **wave** window signal displays, and run a simulation.

## Verifying Generated Code

You can now take the generated code and test bench to an HDL simulator for simulated execution and verification of results. See “Simulating and Verifying Generated HDL Code” on page 2-32 for an example of how to use generated test bench and script files with the Mentor Graphics HDL simulator, ModelSim SE/PE.

## Generating Verilog Model and Test Bench Code

The procedure for generating Verilog code is the same as for generating VHDL code (see “Generating a VHDL Entity from a Subsystem” on page 2-9 and “Generating VHDL Test Bench Code” on page 2-11), except that you should select verilog from the **Language** field of the **HDL Coder** options, as shown in the following figure.



## Simulating and Verifying Generated HDL Code

---

**Note** This section requires the use of the Mentor Graphics HDL simulator, ModelSim SE/PE.

---

This section assumes that you have generated code from the `sfir_fixed` demo model as described in either of the following exercises:

- “Generating HDL Code Using MATLAB Commands” on page 2-6
- “Generating HDL Code in the Simulink GUI” on page 2-15

In this section you compile and run a simulation of the previous generated model and test bench code in ModelSim. The scripts generated by Simulink HDL Coder let you do this with just a few simple commands. The procedure is the same, whether you generated code in the command line environment or in the Simulink environment.

To run the simulation:

- 1** Start ModelSim.
- 2** Set the ModelSim working directory to the directory in which you previously generated code.

```
ModelSim>cd C:/work/sl_hdlcoder_work/hdlsrc
```

- 3** Use the generated compilation script to compile and load the generated model and text bench code. The following listing shows the command and responses from ModelSim.

```
ModelSim>do symmetric_fir_tb_compile.do
# Model Technology ModelSim SE vcom 6.0 Compiler 2004.08 Aug 19 2004
# -- Loading package standard
# -- Loading package std_logic_1164
# -- Loading package numeric_std
# -- Compiling entity symmetric_fir
# -- Compiling architecture rtl of symmetric_fir
# Model Technology ModelSim SE vcom 6.0 Compiler 2004.08 Aug 19 2004
```

```

# -- Loading package standard
# -- Loading package std_logic_1164
# -- Loading package numeric_std
# -- Compiling package symmetric_fir_tb_pkg
# -- Compiling package body symmetric_fir_tb_pkg
# -- Loading package symmetric_fir_tb_pkg
# -- Loading package symmetric_fir_tb_pkg
# -- Compiling entity symmetric_fir_tb
# -- Compiling architecture rtl of symmetric_fir_tb
# -- Loading entity symmetric_fir
    
```

- 4** Use the generated simulation script to execute the simulation. The following listing shows the command and responses from ModelSim. The warning messages are benign.

```

ModelSim>do symmetric_fir_tb_sim.do
# vsim work.symmetric_fir_tb
# Loading C:\Applications\ModelTech_6_0\win32/./std.standard
# Loading C:\Applications\ModelTech_6_0\win32/./ieee.std_logic_1164(body)
# Loading C:\Applications\ModelTech_6_0\win32/./ieee.numeric_std(body)
# Loading work.symmetric_fir_tb_pkg(body)
# Loading work.symmetric_fir_tb(rtl)
# Loading work.symmetric_fir(rtl)
# ** Warning: NUMERIC_STD."<": metavalue detected, returning FALSE
#   Time: 0 ns   Iteration: 0   Instance: /symmetric_fir_tb
.
.
.
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
#   Time: 0 ns   Iteration: 1   Instance: /symmetric_fir_tb
# ** Note: *****TEST COMPLETED *****
#   Time: 140 ns   Iteration: 1   Instance: /symmetric_fir_tb
    
```

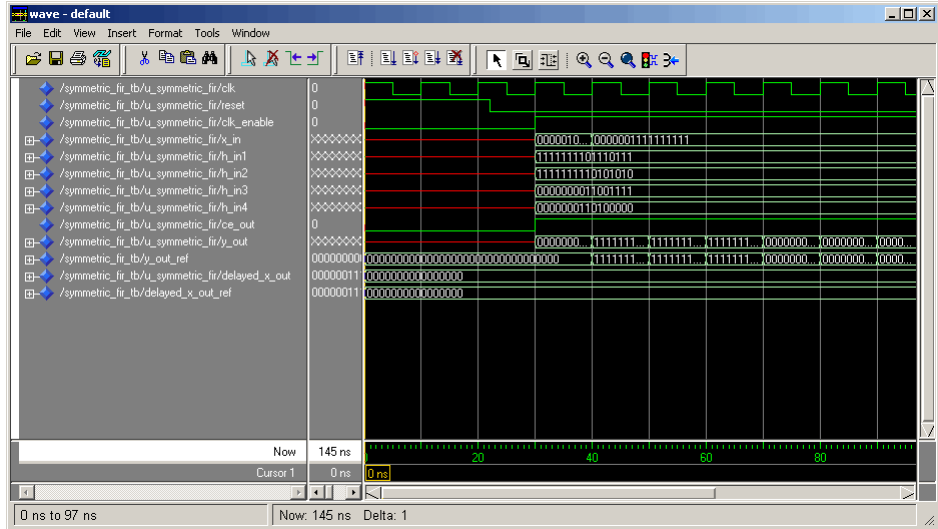
The test bench termination message indicates that the simulation has run to completion successfully, without any comparison errors.

```

# ** Note: *****TEST COMPLETED *****
    
```

- 5** The simulation script displays all inputs and outputs in the model (including the reference signals `y_out_ref` and `delayed_x_out_ref` )

in the ModelSim **wave** window. The following figure shows the signals displayed in the **wave** window.



- 6 Exit ModelSim when you are through viewing signals.
- 7 Close any files you have opened in the MATLAB editor. Then, click the Go Up One Level button in the Current Directory browser, to set the current directory back to your s1\_hdlcoder\_work directory.

# Code Generation Options in the Simulink HDL Coder GUI

---

Viewing and Setting HDL Coder Options (p. 3-2)

How to access HDL options in the Simulink Configuration Parameters dialog box and Model Explorer; the HDL Coder context menu; pointers to related information

HDL Coder Pane: General (p. 3-6)

Controls and options that initiate code generation and compatibility checking, and set parameters that affect overall operation of code generation

HDL Coder Pane: Global Settings (p. 3-13)

Options that specify detailed characteristics of the generated code, including optimizations

HDL Coder Pane: Test Bench (p. 3-45)

Options that specify characteristics of the generated test bench code

HDL Coder Pane: EDA Tool Scripts (p. 3-54)

Options that control generation of script files for third-party HDL simulation and synthesis tools

## Viewing and Setting HDL Coder Options

### In this section...

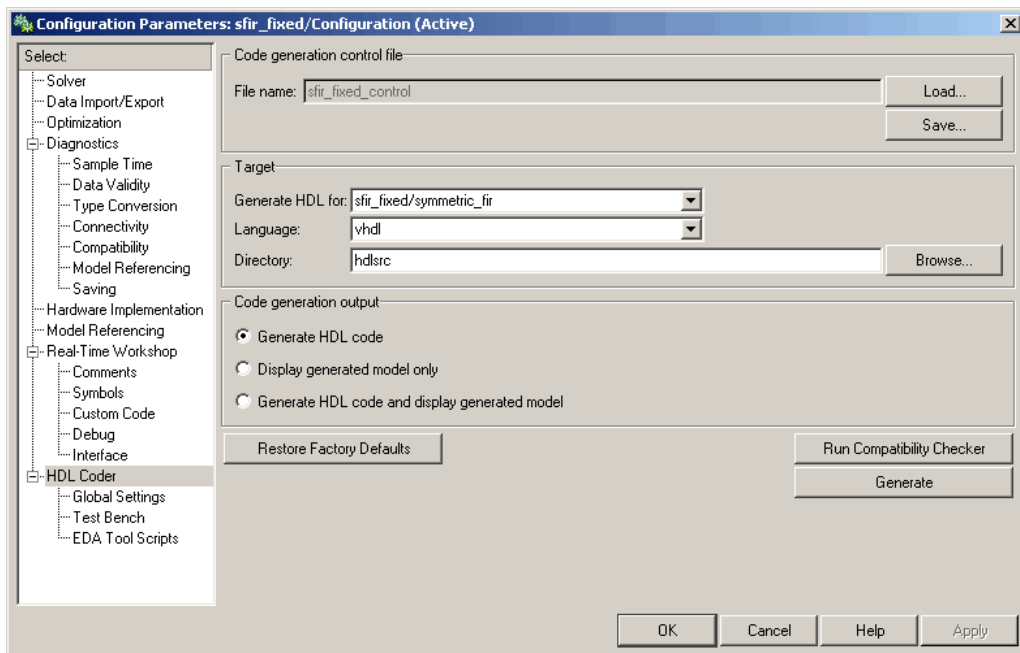
“HDL Coder Options in the Configuration Parameters Dialog Box” on page 3-2

“HDL Coder Options in the Model Explorer” on page 3-3

“HDL Coder Menu” on page 3-4

## HDL Coder Options in the Configuration Parameters Dialog Box

The following figure shows the top-level **HDL Coder** pane as displayed in the Configuration Parameters dialog box. To open this dialog box, select **Simulation > Configuration Parameters** in the Simulink window. Then select **HDL Coder** from the list on the left.



If you are not familiar with Simulink configuration sets and how to view and edit them in the Configuration Parameters dialog box, see the “Configuration Sets” and “Configuration Parameters Dialog Box” sections of the Simulink documentation.

---

**Note** When the **HDL Coder** pane of the Configuration Parameters dialog box is displayed, clicking the **Help** button displays general help for the Configuration Parameters dialog box.

---

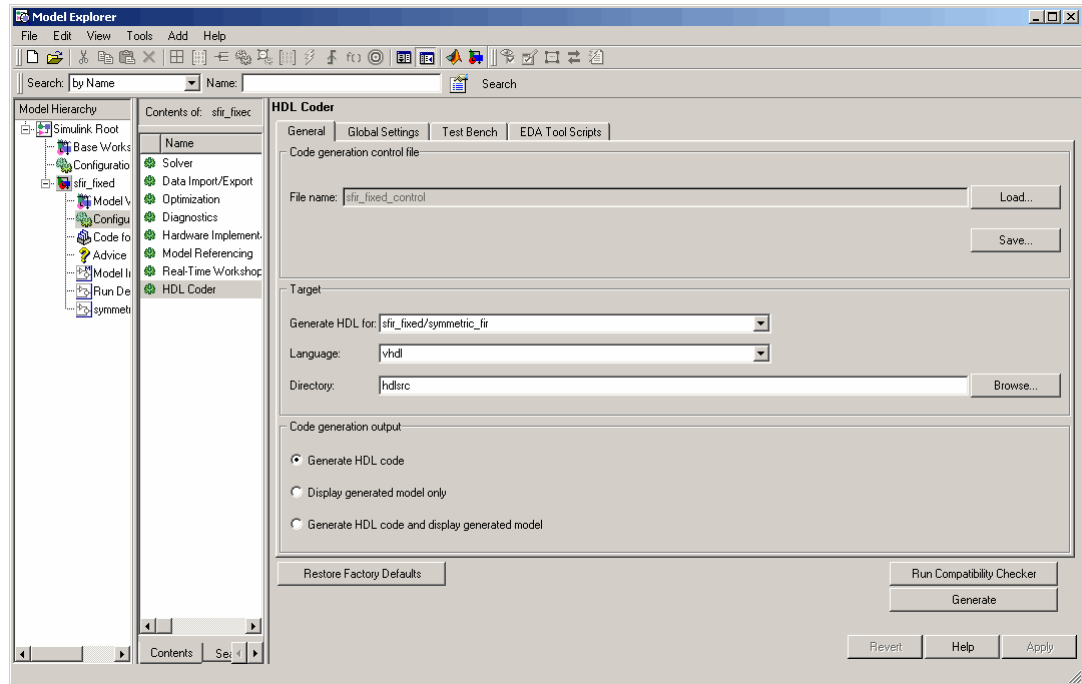
## **HDL Coder Options in the Model Explorer**

The following figure shows the top-level **HDL Coder** pane as displayed in the **Dialog** pane of the Model Explorer.

To view this dialog box:

- 1** Select **View > Model Explorer** in the Simulink window.
- 2** Select your model’s active configuration set in the **Model Hierarchy** tree on the left.
- 3** Select **HDL Coder** from the list in the **Contents** pane.

### 3 Code Generation Options in the Simulink HDL Coder GUI



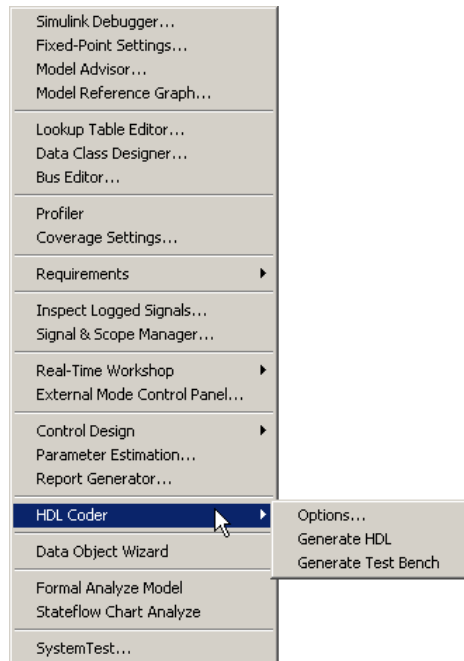
When the **HDL Coder** pane is selected in the Model Explorer, clicking the **Help** button displays the documentation specific to the current tab.

If you are not familiar with the Model Explorer, see “Exploring, Searching, and Browsing Models” in the Simulink documentation.

### HDL Coder Menu

The **HDL Coder** submenu of the Simulink **Tools** menu (see the following figure) provides shortcuts to the HDL code generation options. You can also use this menu to initiate code generation.

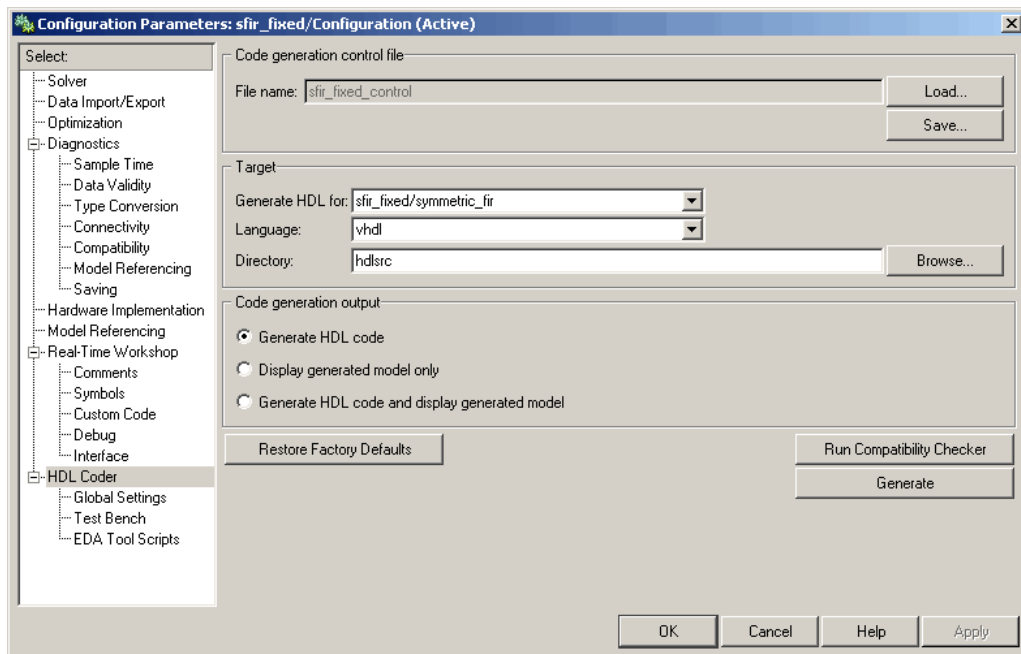




The **HDL Coder** submenu options are:

- **Options:** Open the **HDL Coder** pane in the Configuration Parameters dialog box.
- **Generate HDL:** Initiate HDL code generation; equivalent to the **Generate** button in the Configuration Parameters dialog box or Model Explorer.
- **Generate Test Bench:** Initiate test bench code generation; equivalent to the **Generate Test Bench** button in the Configuration Parameters dialog box or Model Explorer. If you do not select a subsystem from the top (root) level of the current Simulink model in the **Generate HDL for** menu, the **Generate Test Bench** menu option is disabled.

## HDL Coder Pane: General



### In this section...

“HDL Coder Top-Level Pane Overview” on page 3-7

“File name” on page 3-8

“Generate HDL for” on page 3-9

“Language” on page 3-10

“Directory” on page 3-11

“Code Generation Output” on page 3-12

## HDL Coder Top-Level Pane Overview

The top-level **HDL Coder** pane contains buttons that initiate code generation and compatibility checking, and sets parameters that affect overall operation of code generation.

### Buttons in the HDL Coder Top-Level Pane

The buttons in the **HDL Coder** pane perform important functions related to code generation and control file linkage and maintenance. These buttons are:

**Generate:** Initiates code generation for the system selected in the **Generate HDL for** menu. See also `makehdl`.

**Run Compatibility Checker:** Invokes the compatibility checker to examine the system selected in the **Generate HDL for** menu for any compatibility problems. See also `checkhdl`.

**Browse:** Lets you navigate to and select the target directory to which generated code and script files are written. The path to the target directory is entered into the **Target directory** field.

**Load:** Opens a standard file selection dialog box so that you can navigate to and select a control file and load it into memory. See also *Using Control Files in the Code Generation Process*.

**Save:** Opens a standard file save dialog box so that you can save current Simulink HDL Coder settings to a specified control file. See also *Using Control Files in the Code Generation Process*.

**Restore Factory Defaults:** clears the **File Name** field and unlinks the current control file from the model. See also *Using Control Files in the Code Generation Process*.

### File name

Displays the path and file name of the currently selected control file (if any). This is a display-only field.

### Settings

**Default:** No control file name displayed.

- To select a control file, click **Load**, navigate to the desired control file, and select it. The **File Name** field displays the path to the selected file.
- To clear the **File Name** field and unlink the current control file, click the **Restore Factory Defaults** button.

### Command-Line Information

**Property:** HDLControlFiles

**Type:** string

**Value:** Pass in a cell array containing a string that specifies a control file to be attached to the current model.

**Default:** No control file is specified.

### See Also

Using Control Files in the Code Generation Process

## **Generate HDL for**

Select the subsystem or model from which code is generated. The list includes the Simulink path to the root model and to all root-level subsystems in the model.

### **Settings**

**Default:** The root model is selected.

### **Command-Line Information**

Pass in the Simulink path to the model or subsystem for which code is to be generated as the first argument to `makehdl`.

### **See Also**

`makehdl`

### Language

Select the language (VHDL or Verilog) in which code is generated. The selected language is referred to as the target language.

### Settings

**Default:** vhd1

vhd1  
Generate VHDL code.

verilog  
Generate Verilog code.

### Command-Line Information

**Property:** TargetLanguage

**Type:** string

**Value:** 'vhd1' | 'verilog'

**Default:** 'vhd1'

### See Also

- TargetLanguage
- makehdl

## Directory

Enter a path to the directory into which code is generated. Alternatively, click **Browse** to navigate to and select a directory. The selected directory is referred to as the target directory.

## Settings

**Default:** The default target directory is a subdirectory of your working directory, named `hdlsrc`.

## Command-Line Information

**Property:** `TargetDirectory`

**Type:** `string`

**Value:** A valid path to your target directory

**Default:** `'hdlsrc'`

## See Also

- `TargetDirectory`
- `makehdl`

### Code Generation Output

This radio button group contains options related to the creation and display of generated models. Click the desired button to select an option.

#### Settings

**Default: Generate HDL code**

- **Generate HDL code:** Generate HDL code without displaying the generated model.
- **Display generated model only:** Display the generated model without generating HDL code.
- **Generate HDL Code and display generated model:** Display the generated model after HDL code generation completes.

#### Command-Line Information

**Property:** CodeGenerationOutput

**Type:** string

**Value:** 'GenerateHDLCode' |  
'GenerateHDLCodeAndDisplayGeneratedModel' |  
'DisplayGeneratedModelOnly'

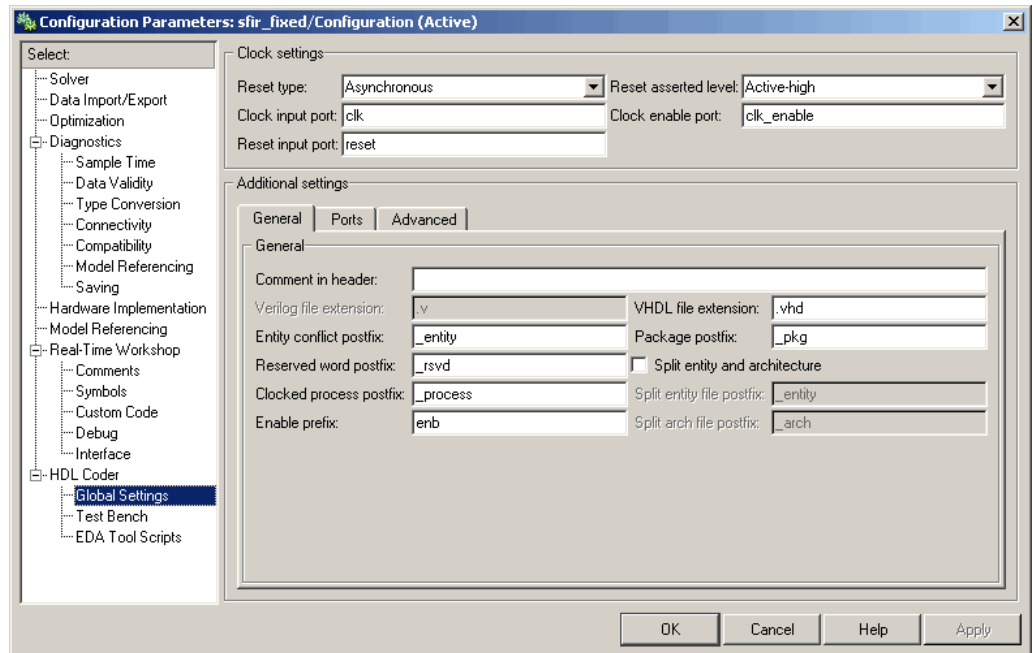
**Default:** 'GenerateHDLCode'

#### See Also

Defaults and Options for Generated Models



## HDL Coder Pane: Global Settings



### In this section...

“Global Settings Overview” on page 3-15

“Reset type” on page 3-16

“Reset asserted level” on page 3-17

“Clock input port” on page 3-18

“Clock enable port” on page 3-19

“Reset input port” on page 3-20

“Comment in header” on page 3-21

“Verilog file extension” on page 3-22

“VHDL file extension” on page 3-23

“Entity conflict postfix” on page 3-24

**In this section...**

- “Package postfix” on page 3-25
- “Reserved word postfix” on page 3-26
- “Split entity and architecture” on page 3-27
- “Split entity file postfix” on page 3-29
- “Split arch file postfix” on page 3-30
- “Clocked process postfix” on page 3-31
- “Enable prefix” on page 3-32
- “Input data type” on page 3-33
- “Output data type” on page 3-34
- “Clock enable output port” on page 3-36
- “Represent constant values by aggregates” on page 3-37
- “Use "rising\_edge" for registers” on page 3-39
- “Loop unrolling” on page 3-40
- “Cast before sum” on page 3-41
- “Use Verilog `timescale directives” on page 3-42
- “Inline VHDL configuration” on page 3-43
- “Concatenate type safe zeros” on page 3-44

## **Global Settings Overview**

The **Global Settings** pane lets you set options to specify detailed characteristics of the generated code, such as HDL element naming and whether certain optimizations are applied.

### **Reset type**

Specifies whether to use asynchronous or synchronous reset logic when generating HDL code for registers.

### **Settings**

**Default:** Asynchronous

Asynchronous

Use asynchronous reset logic.

Synchronous

Use synchronous reset logic.

### **Command-Line Information**

**Property:** ResetType

**Type:** string

**Value:** 'async' | 'sync'

**Default:** 'async'

### **See Also**

ResetType

## Reset asserted level

Specify whether the asserted (active) level of reset input signal is active-high or active-low.

### Settings

**Default:** Active-high

Active-high

Asserted (active) level of reset input signal is active-high (1).

Active-low

Asserted (active) level of reset input signal is active-low (0).

### Command-Line Information

**Property:** ResetAssertedLevel

**Type:** string

**Value:** 'active-high' | 'active-low'

**Default:** 'active-high'

### See Also

ResetAssertedLevel

### Clock input port

Specify the name for the clock input port in generated HDL code.

#### Settings

**Default:** clk

Enter a string value to be used as the clock signal name in generated HDL code. If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`.

#### Command-Line Information

**Property:** ClockInputPort

**Type:** string

**Value:** Any identifier that is legal in the target language

**Default:** 'clk'

#### See Also

ClockInputPort

## Clock enable port

Specify the name for the clock enable port in generated HDL code.

### Settings

**Default:** `clk_enable`

Enter a string value to be used as the clock enable port name in generated HDL code. If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`.

### Tip

The clock enable signal is asserted active-high (1). Thus, the input value must be high for the generated entity's registers to be updated.

### Command-Line Information

**Property:** `ClockEnableInputPort`

**Type:** `string`

**Value:** Any identifier that is legal in the target language

**Default:** `'clk_enable'`

### See Also

`ClockEnableInputPort`

### Reset input port

Enter the name for the reset input port in generated HDL code.

#### Settings

**Default:** reset

Enter a string value to be used as the reset input port name in generated HDL code. If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`.

#### Tips

If the reset asserted level is set to active-high, the reset input signal is asserted active-high (1) and the input value must be high (1) for the entity's registers to be reset. If the reset asserted level is set to active-low, the reset input signal is asserted active-low (0) and the input value must be low (0) for the entity's registers to be reset.

#### Command-Line Information

**Property:** ResetInputPort

**Type:** string

**Value:** Any identifier that is legal in the target language

**Default:** 'reset'

#### See Also

ResetInputPort



## Comment in header

Specify comment lines in header of generated HDL and test bench files.

### Settings

#### No Default

Text entered in this field generates a comment line in the header of generated model and test bench files. The code generator adds leading comment characters as appropriate for the target language. When newlines or linefeeds are included in the string, the code generator emits single-line comments for each newline.

### Command-Line Information

**Property:** UserComment

**Type:** string

### See Also

UserComment

### Verilog file extension

Specify the file-name extension for generated Verilog files.

#### Settings

**Default:** `.v`

This field specifies the file-name extension for generated Verilog files.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is Verilog.

#### Command-Line Information

**Property:** `VerilogFileExtension`

**Type:** `string`

**Default:** `' .v '`

#### See Also

`VerilogFileExtension`

## VHDL file extension

Specify the file-name extension for generated VHDL files.

### Settings

**Default:** .vhd

This field specifies the file-name extension for generated VHDL files.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** VHDLFileExtension

**Type:** string

**Default:** '.vhd'

VHDLFileExtension

### Entity conflict postfix

Specify the string used to resolve duplicate VHDL entity or Verilog module names in generated code.

#### Settings

**Default:** `_entity`

The specified postfix resolves duplicate VHDL entity or Verilog module names. For example, in the default case, if Simulink HDL Coder detects two entities with the name `MyFilt`, the coder names the first entity `MyFilt` and the second instance `MyFilt_entity`.

#### Command-Line Information

**Property:** `EntityConflictPostfix`

**Type:** `string`

**Value:** Any string that is legal in the target language

**Default:** `'_entity'`

#### See Also

`EntityConflictPostfix`

## Package postfix

Specify a string to append to the model or subsystem name to form name of a VHDL package file.

### Settings

**Default:** `_pkg`

Simulink HDL Coder applies this option only if a package file is required for the design.

### Dependency

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** `PackagePostfix`

**Type:** `string`

**Value:** Any string value that is legal in a VHDL package file name

**Default:** `'_pkg'`

### See Also

`PackagePostfix`

### Reserved word postfix

Specify a string to append to value names, postfix values, or labels that are VHDL or Verilog reserved words.

#### Settings

**Default:** `_rsvd`

The reserved word postfix is applied to identifiers (for entities, signals, constants, or other model elements) that conflict with VHDL or Verilog reserved words. For example, if your generating model contains a signal named `mod`, Simulink HDL Coder adds the postfix `_rsvd` to form the name `mod_rsvd`.

#### Command-Line Information

**Property:** `ReservedWordPostfix`

**Type:** `string`

**Default:** `'_rsvd'`

#### See Also

`ReservedWordPostfix`

## Split entity and architecture

Specify whether generated VHDL entity and architecture code is written to a single VHDL file or to separate files.

### Settings

**Default:** Off



On

VHDL entity and architecture definitions are written to separate files.



Off

VHDL entity and architecture code is written to a single VHDL file.

### Tips

The names of the entity and architecture files derive from the base file name (as specified by the generating model or subsystem name). By default, postfix strings identifying the file as an entity (`_entity`) or architecture (`_arch`) are appended to the base file name. You can override the default and specify your own postfix string.

For example, instead of all generated code residing in `MyFIR.vhd`, you can specify that the code reside in `MyFIR_entity.vhd` and `MyFIR_arch.vhd`.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is Verilog.

Selecting this option enables the following parameters:

- **Split entity file postfix**
- **Split architecture file postfix**

### Command-Line Information

**Property:** SplitEntityArch

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

**See Also**

SplitEntityArch



## Split entity file postfix

Enter a string to be appended to the model name to form the name of a generated VHDL entity file.

### Settings

**Default:** `_entity`

### Dependencies

This parameter is enabled by **Split entity and architecture**.

### Command-Line Information

**Property:** `SplitEntityFilePostfix`

**Type:** `string`

**Default:** `'_entity'`

### See Also

`SplitEntityFilePostfix`

### Split arch file postfix

Enter a string to be appended to the model name to form the name of a generated VHDL architecture file.

#### Settings

**Default:** `_arch`

#### Dependencies

This parameter is enabled by **Split entity and architecture**.

#### Command-Line Information

**Property:** `SplitArchFilePostfix`

**Type:** `string`

**Default:** `'_arch'`

#### See Also

`SplitArchFilePostfix`

## Clocked process postfix

Specify a string to append to HDL clock process names.

### Settings

**Default:** `_process`

Simulink HDL Coder uses process blocks for register operations. The label for each of these blocks is derived from a register name and the postfix `_process`. For example, the coder derives the label `delay_pipeline_process` from the register name `delay_pipeline` and the default postfix string `_process`.

### Command-Line Information

**Property:** `ClockProcessPostfix`

**Type:** `string`

**Default:** `'_process'`

### See Also

`ClockProcessPostfix`

## Enable prefix

Specify the base name string for internal clock enables and other flow control signals in generated code.

### Settings

**Default:** 'enb'

Where only a single clock enable is generated, **Enable prefix** specifies the signal name for the internal clock enable signal.

In some cases, multiple clock enables are generated (for example, when a cascade block implementation for certain blocks is specified). In such cases, **Enable prefix** specifies a base signal name for the first clock enable that is generated. For other clock enable signals, numeric tags are appended to **Enable prefix** to form unique signal names. For example, the following code fragment illustrates two clock enables that were generated when **Enable prefix** was set to 'test\_clk\_enable':

```
COMPONENT Timing_Controller
  PORT( clk           : IN   std_logic;
        reset        : IN   std_logic;
        clk_enable    : IN   std_logic;
        test_clk_enable : OUT  std_logic;
        test_clk_enable_5_1_0 : OUT  std_logic
  );
END COMPONENT;
```

### Command-Line Information

**Property:** EnablePrefix

**Type:** string

**Default:** 'enb'

### See Also

EnablePrefix

## Input data type

Specify the HDL data type for the model's input ports.

### Settings

For VHDL, the options are:

**Default:** `std_logic_vector`

`std_logic_vector`

Specifies VHDL type `STD_LOGIC_VECTOR`.

`signed/unsigned`

Specifies VHDL type `SIGNED` or `UNSIGNED`.

For Verilog the options are

**Default:** `wire`

In generated Verilog code, the data type for all ports is `'wire'`. Therefore, **Input data type** is disabled when the target language is Verilog.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** `InputType`

**Type:** `string`

**Value:** (for VHDL) `'std_logic_vector'` | `'signed/unsigned'`  
(for Verilog) `'wire'`

**Default:** (for VHDL) `'std_logic_vector'`  
(for Verilog) `'wire'`

### See Also

`InputType`

### Output data type

Specify the HDL data type for the model's output ports.

#### Settings

For VHDL, the options are:

**Default:** Same as input data type

Same as input data type

Specifies that output ports have the same type specified by **Input data type**.

`std_logic_vector`

Specifies VHDL type `STD_LOGIC_VECTOR`.

`signed/unsigned`

Specifies VHDL type `SIGNED` or `UNSIGNED`.

For Verilog the options are:

**Default:** `wire`

In generated Verilog code, the data type for all ports is `'wire'`. Therefore, **Output data type** is disabled when the target language is Verilog.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** `OutputType`

**Type:** `string`

**Value:** (for VHDL) `'std_logic_vector' | 'signed/unsigned'`  
(for Verilog) `'wire'`

**Default:** If the property is left unspecified, output ports have the same type specified by `InputType`.

**See Also**

OutputType

### **Clock enable output port**

Specify the name for the generated clock enable output.

#### **Settings**

**Default:** `ce_out`

A clock enable output is generated when the design requires one.

#### **Command-Line Information**

**Property:** `ClockEnableOutputPort`

**Type:** `string`

**Default:** `'ce_out'`

#### **See Also**

`ClockEnableOutputPort`



## Represent constant values by aggregates

Specify whether all constants in VHDL code are represented by aggregates, including constants that are less than 32 bits.

### Settings

**Default:** Off



On

The coder represents all constants as aggregates. The following VHDL constant declarations show scalars less than 32 bits being declared as aggregates:

```
CONSTANT coeff1 :signed(15 DOWNT0 0) := (4 DOWNT0 2 => '0', 0 =>'0', OTHERS => ', ');
CONSTANT coeff2 :signed(15 DOWNT0 0) := (6 => '0', 4 DOWNT0 3 => '0', OTHERS => ', ');
```



Off

The coder represents constants less than 32 bits as scalars and constants greater than or equal to 32 bits as aggregates. The following VHDL constant declarations are examples of declarations generated by default for values less than 32 bits:

```
CONSTANT coeff1 :signed(15 DOWNT0 0) := to_signed(-30, 16); -- sfix16_En15
CONSTANT coeff2 :signed(15 DOWNT0 0) := to_signed(-89, 16); -- sfix16_En15
```

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** UseAggregatesForConst

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

**See Also**

UseAggregatesForConst

## Use "rising\_edge" for registers

Specify whether or not generated code uses the VHDL `rising_edge` function to check for rising edges when operating on registers.

### Settings

**Default:** Off



On

Generated code uses the VHDL `rising_edge` function to check for rising edges when operating on registers.



Off

Generated code checks for clock events when operating on registers.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** UseRisingEdge

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

UseRisingEdge

### Loop unrolling

Specify whether VHDL FOR and GENERATE loops are unrolled and omitted from generated VHDL code.

#### Settings

**Default:**Off



On

Unroll and omit FOR and GENERATE loops from the generated VHDL code. (In Verilog code, loops are always unrolled.)



Off

Include FOR and GENERATE loops in the generated VHDL code.

#### Tips

If you are using an electronic design automation (EDA) tool that does not support GENERATE loops, select this option to omit loops from your generated VHDL code.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** LoopUnrolling

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

LoopUnrolling

## Cast before sum

Specify whether operands in addition and subtraction operations are type cast to the result type before executing the operation.

### Settings

**Default:**On



On

Typecast input values in addition and subtraction operations to the result type before operating on the values.



Off

Preserve the types of input values during addition and subtraction operations and then convert the result to the result type.

### Command-Line Information

**Property:** CastBeforeSum

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

CastBeforeSum

## Use Verilog ``timescale` directives

Specify use of compiler ``timescale` directives in generated Verilog code.

### Settings

**Default:** On



On

Use compiler ``timescale` directives in generated Verilog code.



Off

Suppress the use of compiler ``timescale` directives in generated Verilog code.

### Tips

The ``timescale` directive provides a way of specifying different delay values for multiple modules in a Verilog file. This setting does not affect the generated test bench.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is Verilog.

### Command-Line Information

**Property:** UseVerilogTimescale

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

UseVerilogTimescale

## Inline VHDL configuration

Specify whether generated VHDL code includes inline configurations.

### Settings

**Default:** On

On

Include VHDL configurations in any file that instantiates a component.

Off

Suppress the generation of configurations and require user-supplied external configurations. Use this setting if you are creating your own VHDL configuration files.

### Tips

HDL configurations can be either inline with the rest of the VHDL code for an entity or external in separate VHDL source files. By default, Simulink HDL Coder includes configurations for a model within the generated VHDL code. If you are creating your own VHDL configuration files, suppress the generation of inline configurations.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** InlineConfigurations

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

InlineConfigurations

### Concatenate type safe zeros

Specify use of syntax for concatenated zeros in generated VHDL code.

#### Settings

**Default:** On



On

Use the type-safe syntax, '0' & '0', for concatenated zeros. Typically, this syntax is preferred.



Off

Use the syntax "000000..." for concatenated zeros. This syntax can be easier to read and more compact, but it can lead to ambiguous types.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** SafeZeroConcat

**Type:** string

**Value:** 'on' | 'off'

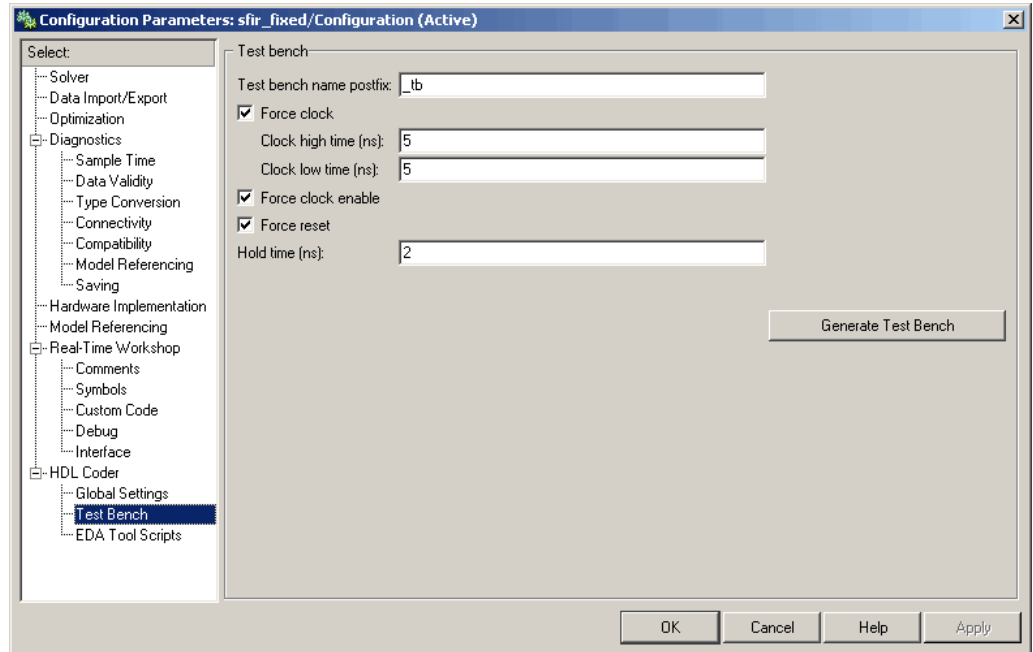
**Default:** 'on'

#### See Also

SafeZeroConcat



## HDL Coder Pane: Test Bench



### In this section...

- “Test Bench Overview” on page 3-46
- “Test bench name postfix” on page 3-47
- “Force clock enable” on page 3-48
- “Force clock” on page 3-49
- “Clock high time (ns)” on page 3-50
- “Clock low time (ns)” on page 3-51
- “Force reset” on page 3-52
- “Hold time (ns)” on page 3-53

### **Test Bench Overview**

The **Test Bench** pane lets you set options that determine characteristics of generated test bench code.

### **Generate Test Bench Button**

The **Generate Test Bench** button initiates test bench generation for the system selected in the **Generate HDL for** menu. See also `makehdltb`.

## Test bench name postfix

Specify a suffix appended to the test bench name.

### Settings

**Default:** `_tb`

For example, if the name of your DUT is `my_test`, Simulink HDL Coder adds the default postfix `_tb` to form the name `my_test_tb`.

### Command-Line Information

**Property:** `TestBenchPostFix`

**Type:** `string`

**Default:** `'_tb'`

### See Also

`TestBenchPostFix`

## Force clock enable

Specify whether the test bench forces clock enable input signals.

### Settings

**Default:** On



On

The test bench forces the clock enable input signals to active-high (1) or active-low (0), depending on the setting of the clock enable input value.



Off

A user-defined external source forces the clock enable input signals.

### Command-Line Information

**Property:** ForceClockEnable

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

ForceClockEnable

## Force clock

Specify whether the test bench forces clock input signals.

### Settings

**Default:** On



On

The test bench forces the clock input signals. When this option is selected, the clock high and low time settings control the clock waveform.



Off

A user-defined external source forces the clock input signals.

### Dependencies

This property enables the **Clock high time** and **Clock high time** options.

### Command-Line Information

**Property:** ForceClock

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

ForceClock

### **Clock high time (ns)**

Specify the period, in nanoseconds, during which the test bench drives clock input signals high (1).

#### **Settings**

**Default:** 5

The **Clock high time** and **Clock low time** properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.

#### **Dependencies**

This parameter is enabled when **Force clock** is selected.

#### **Command-Line Information**

**Property:** ClockHighTime

**Type:** integer

**Default:** 5

#### **See Also**

ClockHighTime

## Clock low time (ns)

Specify the period, in nanoseconds, during which the test bench drives clock input signals low (0).

### Settings

**Default:** 5

The **Clock high time** and **Clock low time** properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.

### Dependencies

This parameter is enabled when **Force clock** is selected.

### Command-Line Information

**Property:** ClockLowTime

**Type:** integer

**Default:** 5

### See Also

ClockLowTime

### Force reset

Specify whether the test bench forces reset input signals.

#### Settings

**Default:** On

On

The test bench forces the reset input signals.

Off

A user-defined external source forces the reset input signals.

#### Tips

If you select this option, you can use the **Hold time** option to control the timing of a reset.

#### Command-Line Information

**Property:** ForceReset

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

ForceReset



## Hold time (ns)

Specify a hold time, in nanoseconds, for input signals and forced reset input signals.

### Settings

**Default:** 2

The hold time defines the number of nanoseconds (expressed as a positive integer) that reset input signals and input data are held past the clock rising edge.

### Tips

This option applies to reset input signals only if **Force reset** is selected.

### Command-Line Information

**Property:** HoldTime

**Type:** integer

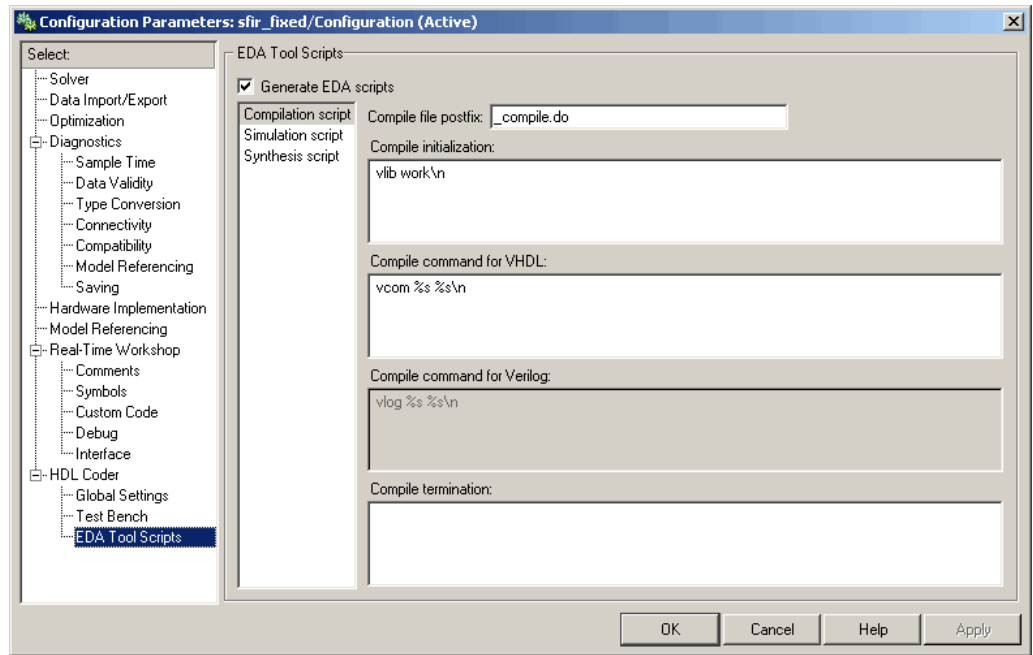
**Value:** A positive integer

**Default:** 2

### See Also

HoldTime

## HDL Coder Pane: EDA Tool Scripts



### In this section...

- “EDA Tool Scripts Overview” on page 3-56
- “Generate EDA scripts” on page 3-57
- “Compile file postfix” on page 3-58
- “Compile Initialization” on page 3-59
- “Compile command for VHDL” on page 3-60
- “Compile command for Verilog” on page 3-61
- “Compile termination” on page 3-62
- “Simulation file postfix” on page 3-63
- “Simulation initialization” on page 3-64
- “Simulation command” on page 3-65

**In this section...**

“Simulation waveform viewing command” on page 3-66

“Simulation termination” on page 3-67

“Synthesis file postfix” on page 3-68

“Synthesis initialization” on page 3-69

“Synthesis command” on page 3-70

“Synthesis termination” on page 3-71

### **EDA Tool Scripts Overview**

The **EDA Tool Scripts** pane lets you set all options that control generation of script files for third-party HDL simulation and synthesis tools.

## Generate EDA scripts

Enable generation of script files for third-party electronic design automation (EDA) tools. These scripts let you compile and simulate generated HDL code and/or synthesize generated HDL code.

### Settings

**Default:** On



On

Generation of script files is enabled.



Off

Generation of script files is disabled.

### Command-Line Information

**Parameter:** EDAScriptGeneration

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- EDAScriptGeneration

### Compile file postfix

Specify a postfix string appended to the DUT or test bench name to form the compilation script file name.

#### Settings

**Default:** `_compile.do`

For example, if the name of the device under test or test bench is `my_design`, Simulink HDL Coder adds the postfix `_compile.do` to form the name `my_design_compile.do`.

#### Command-Line Information

**Property:** `HDLCompileFilePostfix`

**Type:** `string`

**Default:** `'_compile.do'`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLCompileFilePostfix`

## Compile Initialization

Specify a format string passed to `fprintf` to write the Init section of the compilation script.

### Settings

**Default:** `vlib work\n`

The Init phase of the script performs any required setup actions, such as creating a design library or a project file.

### Command-Line Information

**Property:** `HDLCompileInit`

**Type:** `string`

**Default:** `'vlib work\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLCompileInit`

## Compile command for VHDL

Specify a format string passed to `fprintf` to write the `Cmd` section of the compilation script for VHDL files.

### Settings

**Default:** `vcom %s %s\n`

The command-per-file phase (`Cmd`) of the script is called iteratively, once per generated HDL file or once per signal. On each call, a different file or signal name is passed in.

The two arguments in the compile command are the contents of the `SimulatorFlags` property and the file name of the current entity or module. To omit the flags, set `SimulatorFlags` to `' '` (the default).

### Command-Line Information

**Property:** `HDLCompileVHDLCmd`

**Type:** `string`

**Default:** `'vcom %s %s\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLCompileVHDLCmd`



## Compile command for Verilog

Specify a format string passed to `fprintf` to write the `Cmd` section of the compilation script for Verilog files.

### Settings

**Default:** `vlog %s %s\n`

The command-per-file phase (`Cmd`) of the script is called iteratively, once per generated HDL file or once per signal. On each call, a different file or signal name is passed in.

The two arguments in the compile command are the contents of the `SimulatorFlags` property and the file name of the current entity or module. To omit the flags, set `SimulatorFlags` property to `' '` (the default).

### Command-Line Information

**Property:** `HDLCompileVerilogCmd`

**Type:** `string`

**Default:** `'vlog %s %s\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLCompileVerilogCmd`

### Compile termination

Specify a format string passed to `fprintf` to write the termination portion of the compilation script.

#### Settings

**Default:** empty string

The termination phase (`Term`) is the final execution phase of the script. One application of this phase is to execute a simulation of HDL code that was compiled in the `Cmd` phase. The `Term` phase takes no arguments.

#### Command-Line Information

**Property:** `HDLCompileTerm`

**Type:** `string`

**Default:** `''`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLCompileTerm`

## Simulation file postfix

Specify a postfix string appended to the DUT or test bench name to form the simulation script file name.

### Settings

**Default:** `_sim.do`

For example, if the name of the device under test or test bench is `my_design`, Simulink HDL Coder adds the postfix `_sim.do` to form the name `my_design_sim.do`.

### Command-Line Information

**Property:** `HDLSimFilePostfix`

**Type:** `string`

**Default:** `'_sim.do'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLSimFilePostfix`

## Simulation initialization

Specify a format string passed to `fprintf` to write the initialization section of the simulation script.

### Settings

**Default:** The default string is

```
[ 'onbreak resume\nonerror resume\n' ]
```

The `Init` phase of the script performs any required setup actions, such as creating a design library or a project file.

### Command-Line Information

**Property:** `HDLSimInit`

**Type:** `string`

**Default:** `[ 'onbreak resume\nonerror resume\n' ]`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLSimInit`

## Simulation command

Specify a format string passed to `fprintf` to write the simulation command.

### Settings

**Default:** `vsim work.%s\n`

The implicit argument is the top-level module or entity name.

### Command-Line Information

**Property:** HDLSimCmd

**Type:** string

**Default:** `'vsim work.%s\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- HDLSimCmd

## Simulation waveform viewing command

Specify the waveform viewing command written to simulation script.

### Settings

**Default:** `add wave sim:%s\n`

The implicit argument is the top-level module or entity name.

### Command-Line Information

**Property:** HDLSimViewWaveCmd

**Type:** string

**Default:** 'add wave sim:%s\n'

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- HDLSimViewWaveCmd

## Simulation termination

Specify a format string passed to `fprintf` to write the termination portion of the simulation script.

### Settings

**Default:** `run -all\n`

The termination phase (`Term`) is the final execution phase of the script. One application of this phase is to execute a simulation of HDL code that was compiled in the `Cmd` phase. The `Term` phase takes no arguments.

### Command-Line Information

**Property:** `HDLSimTerm`

**Type:** `string`

**Default:** `'run -all\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLSimTerm`

### Synthesis file postfix

Specify a postfix string appended to file name for generated Synplify synthesis scripts.

#### Settings

**Default:** `_synplify.tcl`

For example, if the name of the device under test is `my_design`, Simulink HDL Coder adds the postfix `_synplify.tcl` to form the name `my_design_synplify.tcl`.

#### Command-Line Information

**Property:** `HDLSynthFilePostfix`

**Type:** `string`

**Default:** `'_synplify.tcl'`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLSynthFilePostfix`



## Synthesis initialization

Specify a format string passed to `fprintf` to write the initialization section of the synthesis script.

### Settings

**Default:** `project -new %s.prj\n`

The default string is a synthesis project creation command. The implicit argument is the top-level module or entity name.

### Command-Line Information

**Property:** HDLSynthInit

**Type:** string

**Default:** `'project -new %s.prj\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- HDLSynthInit

### Synthesis command

Specify a format string passed to `fprintf` to write the synthesis command.

#### Settings

**Default:** `add_file %s\n`

The implicit argument is the top-level module or entity name.

#### Command-Line Information

**Property:** `HDLSynthCmd`

**Type:** `string`

**Default:** `add_file %s\n`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- `HDLSynthCmd`

## Synthesis termination

Specify a format string passed to `fprintf` to write the termination portion of the synthesis script.

### Settings

#### Default:

```
['set_option -technology VIRTEX4\n',...  
'set_option -part XC4VSX35\n',...  
'set_option -synthesis_onoff_pragma 0\n',...  
'set_option -frequency auto\n',...  
'project -run synthesis\n']
```

The termination phase (Term) is the final execution phase of the script. The Term phase takes no arguments.

### Command-Line Information

**Property:** HDLSynthTerm

**Type:** string

**Default:** ['set\_option -technology VIRTEX4\n', 'set\_option -part XC4VSX35\n', 'set\_option -synthesis\_onoff\_pragma 0\n', 'set\_option -frequency auto\n', 'project -run synthesis\n']

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Panel
- HDLSynthTerm



# Generating HDL Code for Multirate Models

---

Overview (p. 4-2)

Overview of HDL code generation for single-clock, single-tasking multirate models

Configuring Multirate Models for HDL Code Generation (p. 4-3)

Guidelines for setting up multirate models and blocks for HDL code generation

Example: Model With a Multirate DUT (p. 4-6)

Illustrates the timing of computations for a simple multirate model

Properties Supporting Multirate Code Generation (p. 4-8)

Command-line properties related to multirate code generation

### Overview

Simulink HDL Coder supports HDL code generation for single-clock, single-tasking multirate models. Your model can include blocks running at multiple sample rates:

- Within the device under test (DUT).
- In the test bench driving the DUT. In this case, the DUT inherits multiple sample rates from its inputs or outputs.
- In both the test bench and the DUT.

HDL code generated from multirate models employs a single clock. A *timing controller* (`Timing_Controller`) entity generates the required rates from a single master clock using counters and multiple clock enables. The master clock rate (always the fastest rate in the model) is referred to as the *base rate*. The rates generated from the master clock are referred to as *subrates*. The `Timing_Controller` entity definition is written to a separate code file (`Timing_Controller.vhd` or `Timing_Controller.v`).

In general, generating HDL code for a multirate model does not differ greatly from generating HDL code for a single-rate model. However, there are a few requirements and restrictions on the configuration of the model and the use of specialized blocks (such as Rate Transitions) that apply to multirate models. These are discussed in the following sections.

# Configuring Multirate Models for HDL Code Generation

## In this section...

“Overview” on page 4-3

“Configuring Model Parameters” on page 4-3

“Configuring Sample Rates in the Model” on page 4-4

“Constraints for Rate Transition Blocks and Other Blocks in Multirate Models” on page 4-4

## Overview

Certain requirements and restrictions apply to multirate models that are intended for HDL code generation. This section provides guidelines on how to configure model and block parameters to meet these requirements.

## Configuring Model Parameters

Before generating HDL code, configure the parameters of your model using the `hdlsetup` command. This ensures that your multirate model is set up correctly for HDL code generation. This section summarizes settings applied to the model by `hdlsetup` that are relevant to multirate code generation. These include:

- **Solver** options that are recommended or required for HDL code generation:
  - **Type:** Fixed-step.
  - **Solver:** discrete (no continuous states). Other fixed-step solvers could be selected, but this option is usually correct for simulating discrete systems.
  - **Tasking mode:** Must be explicitly set to `SingleTasking`. Do not set **Tasking mode** to `Auto`.
- **Diagnostics / Sample time** options required when generating HDL code for multirate models:
  - **Multitask rate transition:** error
  - **Single task rate transition:** error

In multirate models intended for HDL code generation, Rate Transition blocks must be explicitly inserted when blocks running at different rates are connected. Setting **Multitask rate transition** and **Single task rate transition** to error ensures that any illegal rate transitions are detected before code is generated.

### Configuring Sample Rates in the Model

Simulink HDL Coder requires that at least one valid sample rate (sample time > 0) must exist in the model. If all rates are 0, -1, or -2, the code generator (makehdl) and compatibility checker (checkhdl) terminates with an error message.

### Constraints for Rate Transition Blocks and Other Blocks in Multirate Models

This section describes constraints you should observe when configuring Rate Transition, Upsample, Downsample, Zero-Order Hold, and various types of delay blocks in multirate models intended for HDL code generation.

#### Rate Transition Blocks

Rate Transition blocks must be explicitly inserted into the signal path when blocks running at different rates are connected. For general information about the Rate Transition block, see Rate Transition in the Simulink documentation.

Make sure the data transfer properties for Rate Transition blocks are set as follows:

- **Ensure deterministic data transfer:** Selected.
- **Ensure data integrity during data transfer:** Selected.

#### Upsample

When configuring Upsample blocks, set **Frame based mode** to Maintain input frame size.

When the Upsample block is in this mode, **Initial conditions** has no effect on generated code.



## Downsample

Configure Downsample blocks as follows:

- Set **Frame based mode** to Maintain input frame size.
- Set **Sample based mode** to Allow multirate.

Given these Downsample block settings, **Initial conditions** has no effect on generated code if **Sample offset** is set to 0.

## Delay and Zero-Order Hold Blocks

Use Rate Transition blocks, rather than any of the following block types, to create rate transitions in models intended for HDL code generation:

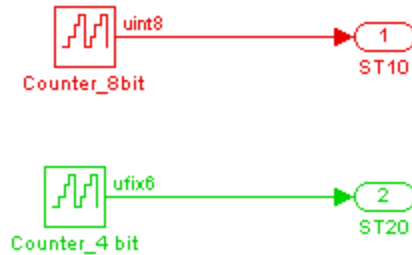
- Unit Delay
- Unit Delay Enabled
- Integer Delay
- Tapped Delay
- Zero-Order Hold

All types of Delay blocks listed should be configured to have the same input and output sample rates.

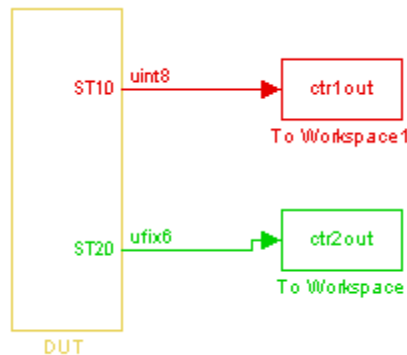
Zero-Order Hold blocks must be configured with inherited (-1) sample times.

## Example: Model With a Multirate DUT

The following block diagram shows the interior of a subsystem containing blocks that are explicitly configured with different sample times. The upper and lower Counter Free-Running blocks have sample times of 10 s and 20 s respectively. The counter output signals are routed to output ports ST10 and ST20, which inherit their sample times. The signal path terminating at ST10 runs at the base rate of the model; the signal path terminating at ST20 is a subrate signal, running at half the base rate of the model.



As shown in the next figure, the outputs of the multirate DUT drive To Workspace blocks in the test bench. These blocks inherit the sample times of the DUT outputs.



The following listing shows the VHDL entity declaration generated for the DUT.

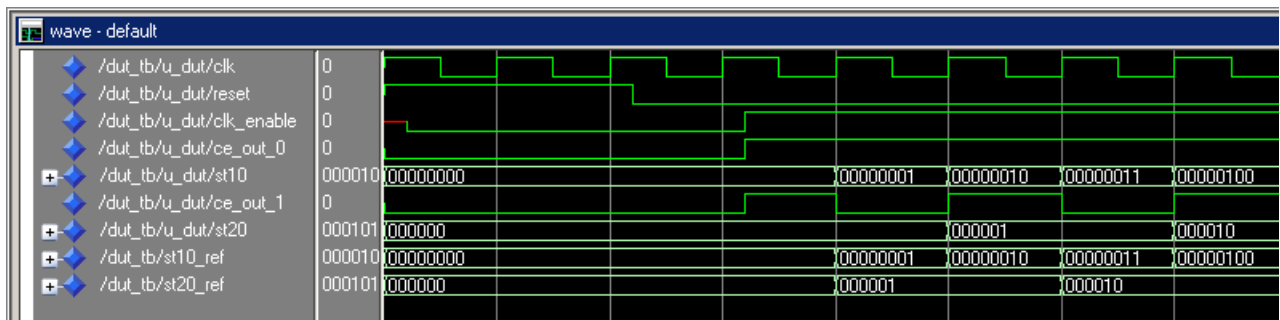
```

ENTITY DUT IS
  PORT( clk
        : IN   std_logic;
        reset
        : IN   std_logic;
        clk_enable
        : IN   std_logic;
        ce_out_0
        : OUT  std_logic;
        ce_out_1
        : OUT  std_logic;
        ST10
        : OUT  std_logic_vector(7 DOWNTO 0); -- uint8
        ST20
        : OUT  std_logic_vector(5 DOWNTO 0) -- ufix6
        );
END DUT;

```

The entity has the standard clock, reset, and clock enable inputs and data outputs for the ST10 and ST20 signals. In addition, the entity has two clock enable outputs (ce\_out\_0 and ce\_out\_1). These clock enable outputs replicate internal clock enable signals maintained by the TimingController entity.

The following screen shot, showing a portion of a ModelSim simulation of the generated VHDL code, lets you observe the timing relationship of the base rate clock (clk), the clock enables, and the computed outputs of the model.



After the assertion of `clk_enable` (replicated by `ce_out_0`), a new value is computed and output to ST10 for every cycle of the base rate clock.

A new value is computed and output for subrate signal ST20 for every other cycle of the base rate clock. An internal signal, `enb_1_2_1` (replicated by `ce_out_1`) governs the timing of this computation.

## Properties Supporting Multirate Code Generation

In this section...
“Overview” on page 4-8
“HoldInputDataBetweenSamples” on page 4-8
“ClockEnableDelay” on page 4-8

### Overview

This section summarizes command-line (makehdl) properties that provide additional control over multirate code generation.

### HoldInputDataBetweenSamples

This property determines how long (in terms of base rate clock cycles) data values for subrate signals are held in a valid state.

When 'on' (the default), data values for subrate signals are held in a valid state across each subrate sample period.

When 'off', data values for subrate signals are held in a valid state for only one base-rate clock cycle. See `HoldInputDataBetweenSamples` for details.

### ClockEnableDelay

This property specifies a delay time  $D$  (a number of base-rate clock cycles) applied to `clk_enable` signals when the model's reset input signal is asserted. This delay time is in addition to the hold time specified by the `HoldTime` property. See `ClockEnableDelay` for details.

# Code Generation Control Files

---

Overview of Control Files (p. 5-3)	Motivation for code generation control files; control file statement types; selectable HDL block implementations, implementation parameters, and implementation mappings
Structure of a Control File (p. 5-6)	Required elements of a control file
Code Generation Control Objects and Methods (p. 5-8)	Instantiating a code generation control object; code generation control object methods that you can invoke in a control file
Using Control Files in the Code Generation Process (p. 5-16)	How to create a control file and save HDL code generation settings, attach or detach a control file to or from your model, and invoke a control file during code generation
Specifying Block Implementations and Parameters in the Control File (p. 5-24)	How block implementations and implementation parameters are specified in a control file; how to use the <code>hdlnewforeach</code> function to generate selection/action statements; summary of blocks with multiple implementations
Summary of Block Implementations (p. 5-35)	Summary of implementations for all supported blocks

Block Implementation Parameters  
(p. 5-47)

Code generation parameters supported for specific block implementations

Restrictions on Use of Blocks in the Test Bench (p. 5-49)

Summarizes restrictions on the use of certain blocksets when deployed in a test bench

## Overview of Control Files

### In this section...

“What is a Control File?” on page 5-3

“Selectable Block Implementations and Implementation Parameters” on page 5-4

“Implementation Mappings” on page 5-5

“Control File Demo” on page 5-5

### What is a Control File?

*Code generation control files* (referred to in this document as *control files*) let you

- Save your model’s Simulink HDL Coder options in a persistent form.
- Extend the HDL code generation process and direct its details.

A control file is an M-file that you attach to your model, using either the `makehdl` command or the Simulink Configuration Parameters dialog box. You do not need to know any internal details of the code generation process to use a control file.

In the current release, control files support the following statement types:

- *Selection/action* statements provide a general framework for the application of different types of transformations to selected model components. Selection/action statements *select* a group of blocks within your model, and specify an *action* to be executed when code is generated for each block in the selected group.

Selection criteria include block type and location within the model. For example, you might select all built-in Gain blocks at or below the level of a certain subsystem within your model.

A typical action applied to such a group of blocks is to direct the code generator to execute a specific *block implementation method* when generating HDL code for the selected blocks. For example, for Gain blocks,

you might choose a method that generates code that is optimized for speed or chip area.

- *Property setting* statements let you
  - Select the model or subsystem from which code is to be generated.
  - Set the values of code generation properties to be passed to the code generator. The properties and syntax are the same as those used for the `makehdl` command.
  - Set up default or template HDL code generation settings for your organization.

## Selectable Block Implementations and Implementation Parameters

Selection/action statements provide a general framework that lets you define how Simulink HDL Coder acts upon selected model components. The current release supports one such action: execution of block implementation methods.

Block implementation methods are code generator components that emit HDL code for the blocks in a Simulink model. This document refers to block implementation methods as *block implementations* or simply *implementations*.

Simulink HDL Coder provides at least one block implementation for every supported block. This is called the *default implementation*. In addition, Simulink HDL Coder provides selectable alternate block implementations for certain block types. Each implementation is optimized for different characteristics, such as speed or chip area. For example, you can choose Gain block implementations that use canonic signed digit (CSD) techniques (reducing area), or use a default implementation that retains multipliers.

For many block implementations, you can set *implementation parameters* that provide a further level of control over how code is generated for a particular implementation. For example, many blocks support the 'OutputPipeline' implementation parameter. This parameter lets you specify the generation of pipeline stages for selected blocks by passing in the required pipeline depth as the parameter value.



## Implementation Mappings

Control files let you specify one or more *implementation mappings* that control how HDL code is to be generated for a specified group of blocks within the model. An implementation mapping is an association between a selected block or set of blocks within the model and a block implementation.

To select the set of blocks to be mapped to a block implementation, you specify

- A `modelscope`: a Simulink block path (which could incorporate an entire model or sublevel of the model, or a specific subsystem or block)
- A `blocktype`: a Simulink block type that corresponds to the selected block implementation

During code generation, each defined `modelscope` is searched for instances of the associated `blocktype`. For each such block instance encountered, the code generator uses the selected block implementation.

## Control File Demo

The “Getting Started with Control Files” demo illustrates the use of simple control files to define implementation mappings and generate Verilog code. The demo is located in the **Demos** pane on the left of the MATLAB Help browser. To run the demo, select **Simulink > Simulink HDL Coder > Getting Started with Control Files** in the **Demos** pane. Then follow the demo instructions.

## Structure of a Control File

The required elements for a code generation control file are as follows:

- A control file is an M-file that implements a single function, which is invoked during the code generation process.

The function must instantiate a *code generation control object*, set its properties, and return the object to the code generator.

Setting up a code generation control object requires the use of a small number of methods, as described in “Code Generation Control Objects and Methods” on page 5-8. You do not need to know internal details of the code generation control object or the class to which it belongs.

The object is constructed using the `hdlnewcontrol` function. The argument to `hdlnewcontrol` is the name of the control file itself. Use the MATLAB `mfilename` function to pass in the file name, as shown in the following example.

```
function c = dct8config
c = hdlnewcontrol(mfilename);

% Set target language for Verilog.
c.set('TargetLanguage','Verilog');

% Set top-level subsystem from which code is generated.
c.generateHDLFor('dct8_fixed/OneD_DCT8');
```

- Following the constructor call, your code will invoke methods of the code generation control object. The previous example calls the `set` and `generateHDLFor` methods. These and all other public methods of the object are discussed in “Code Generation Control Objects and Methods” on page 5-8.
- Your control file must be attached to your Simulink model before code generation, as described in “Using Control Files in the Code Generation Process” on page 5-16. The interface between the code generator and your attached control file is automatic.
- A control file must be located in either the current working directory, or a directory that is in the MATLAB path.

However, your control files should not be located within the MATLAB directory tree because they could be overwritten by subsequent MATLAB installations.

## Code Generation Control Objects and Methods

### In this section...

“Overview” on page 5-8

“hdlnewcontrol” on page 5-8

“forEach” on page 5-8

“forAll” on page 5-14

“set” on page 5-14

“generateHDLFor” on page 5-14

### Overview

Code generation control objects are instances of the class `slhdlcoder.ConfigurationContainer`. This section describes the methods of that class that you can use in your control files. Other methods of this class are for MathWorks internal use only. The methods are described in the following sections:

### hdlnewcontrol

The `hdlnewcontrol` function constructs a code generation control object. The syntax is

```
object = hdlnewcontrol(mfilename);
```

The argument to `hdlnewcontrol` is the name of the control file itself. Use the MATLAB `mfilename` function to pass in the file name string.

### forEach

This method establishes an implementation mapping between an HDL block implementation and a selected block or set of blocks within the model. The syntax is

```
object.forEach({'modelscopes'}, ...  
              'blocktype', {'block_parms'}, ...
```

```
'implementation', {'implementation_parms'})
```

The `forEach` method selects a set of Simulink blocks (`modelscope`s) that is searched, during code generation, for instances of a specified type of block (`blocktype`). Code generation for each block instance encountered uses the HDL block implementation specified by the `implementation` parameter.

---

**Note** You can use the `hdlnewforeach` function to generate `forEach` method calls for insertion into your control files. See “Generating Selection/Action Statements with the `hdlnewforeach` Function” on page 5-25 for more information.

---

The following table summarizes the arguments to the `forEach` method.

Argument	Type	Description
modelscope	String or cell array of strings	<p>Strings defining one or more Simulink paths: <code>{'path1' 'path2' ... 'pathN' }</code></p> <p>Each such path defines a <code>modelscope</code>: a set of Simulink blocks that participate in an implementation mapping. The selected set of blocks in a <code>modelscope</code> could include the entire model, all blocks at a specified level of the model, or a specific block or subsystem. A path terminating in a wildcard character ('*') indicates inclusion of all blocks at or below the model level specified by the path. Supported syntax for <code>modelscope</code> paths is</p> <ul style="list-style-type: none"> <li>• 'model/*': all blocks in the model</li> <li>• 'model/subsyslevel/block': a specific block within a specific level of the model</li> <li>• 'model/subsyslevel/subsystem': a specific subsystem block within a specific level of the model</li> <li>• 'model/subsyslevel/*': any block within a specific level of the model</li> </ul> <p>See also “Resolution of modelscope” on page 5-13.</p>

Argument	Type	Description
blocktype	String	<p>Simulink block specification that identifies the type of block that is to be mapped to the HDL block implementation. The syntax for a block specification is the same as that used in the Simulink <code>add-block</code> command. For built-in Simulink blocks, the <code>blocktype</code> is of the form</p> <pre>'built-in/blockname'</pre> <p>For other blocks, <code>blocktype</code> must include the library containing the block, for example:</p> <pre>'dsparch4/Digital Filter'</pre> <p>If the block is contained in a sublibrary, the full path from the top-level library must be included.</p>
block_parms	Cell array of strings	Reserved for future use; not supported in the current release. Pass in an empty cell array ( <code>{}</code> ) as placeholder.

Argument	Type	Description
implementation	String	<p>An HDL block implementation to be used in code generation for all blocks that meet the <code>modelscope</code> and <code>blocktype</code> search criteria. An implementation is specified in the form <code>package.class</code>, for example:</p> <pre style="text-align: center;">hdldefaults.GainMultHDLEmission</pre> <p>“Specifying Block Implementations and Parameters in the Control File” on page 5-24 lists available implementations.</p>
implementation_parms	Cell array of property/value pairs	<p>Cell array of property/value pairs that set code generation parameters for the block implementation specified by the <code>implementation</code> argument. Parameters are specified as: 'Property', value where 'Property' is the name of the property (string) and value is the value applied to the property. If the implementation does not have any parameters, or you want to use the default parameters, pass in an empty cell array ({}).</p> <p>“Block Implementation Parameters” on page 5-47 describes the syntax of each block implementation parameter, and describes how the parameter affects generated code.</p> <p>“Summary of Block Implementations” on page 5-35 lists all supported blocks and their implementations and parameters.</p> <p>You can use the <code>hdlnewforeach</code> function to obtain the parameter names for any selected block(s) in a model. See “Specifying Block Implementations and Parameters in the Control File” on page 5-24 for an example.</p>



## Resolution of modelscopes

A possible conflict exists in the `forEach` specifications in the following example:

```
% 1. Use default (multipliers) Gain block implementation
% for one specific Gain block within OneD_DCT8 subsystem
c.forEach('dct8_fixed/OneD_DCT8/Gain14',...
    'built-in/Gain', {},...
    'hdldefaults.GainMultHDLEmission');
% 2. Use factored CSD Gain block implementation
% for all Gain blocks at or below level of OneD_DCT8 subsystem.
c.forEach('dct8_fixed/OneD_DCT8/*',...
    'built-in/Gain', {},...
    'hdldefaults.GainFCSDHDLEmission');
```

The first `forEach` call defines an implementation mapping for a specific block within the subsystem `OneD_DCT8`. The second `forEach` call defines a different implementation mapping for all blocks within or below the subsystem `OneD_DCT8`.

Simulink HDL Coder resolves such ambiguities by always giving higher priority to the more specific modelscope. In the example, the `Gain14` block uses the `hdldefaults.GainMultHDLEmission` implementation, while all other blocks within or below the subsystem `OneD_DCT8` use the `hdldefaults.GainFCSDHDLEmission` implementation.

Five levels of modelscope priority from most specific (1) to least specific (5) are defined:

- 1** A/B/C/block
- 2** A/B/C/\*
- 3** A/B/\*
- 4** \*
- 5** Unspecified. Use MathWorks default implementation.

### forAll

This method is a shorthand form of `forEach`. Only one `modelscope` path is specified. The `modelscope` argument is specified as a string (not a cell array) and it is implicitly terminated with `/*`. The syntax is

```
object.forAll('modelscope', ...  
             'blocktype', {'block_parms'}, ...  
             'implementation', {'implementation_parms'})
```

All other arguments are the same as those described for “`forEach`” on page 5-8.

### set

The `set` method sets one or more code generation properties. The syntax is

```
object.set('PropertyName', PropertyValue,...)
```

The argument list specifies one or more code generation options as property/value pairs. You can set any of the code generation properties documented in Chapter 13, “Properties — Alphabetical List”, *except* the `HDLControlFiles` property.

---

**Note** If you specify the same property in both your control file and your `makehdl` command, the property will be set to the value specified in the control file.

Likewise, when generating code via the GUI, if you specify the same property in both your control file and the **HDL Coder** options panes, the property will be set to the value specified in the control file.

---

### generateHDLFor

This method selects the model or subsystem from which code is to be generated. The syntax is

```
object.generateHDLFor('simulinkpath')
```

The argument is a string specifying the full Simulink path to the model or subsystem from which code is to be generated.

Use of this method is optional. You can specify the same parameter in the **Generate HDL for** menu in the **HDL Coder** pane of the Configuration Parameters dialog box, or in a `makehdl` command.

## Using Control Files in the Code Generation Process

In this section...
“Creating a Control File and Saving Your HDL Code Generation Settings” on page 5-16
“Associating an Existing Control File with Your Model” on page 5-19
“Detaching a Control File from Your Model” on page 5-22
“Setting Up HDL Code Generation Defaults With a Control File” on page 5-22

---

### Creating a Control File and Saving Your HDL Code Generation Settings

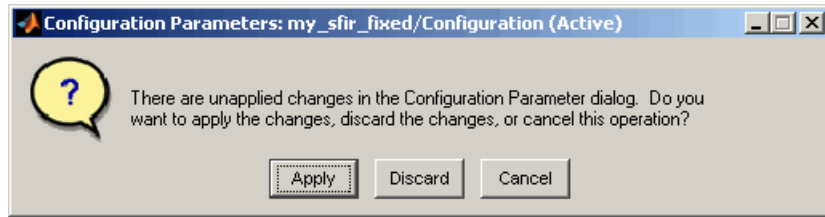
**Note** When you save a Simulink model, your Simulink HDL Coder settings are not saved with the model like other components of the model's configuration set. If you want your Simulink HDL Coder settings to persist across sessions with a model, you must save your current Simulink HDL Coder settings to a control file. The control file is then linked to the model, and the linkage is preserved when you save the model.

---

#### Saving Your HDL Coder Generation Settings to a Control File

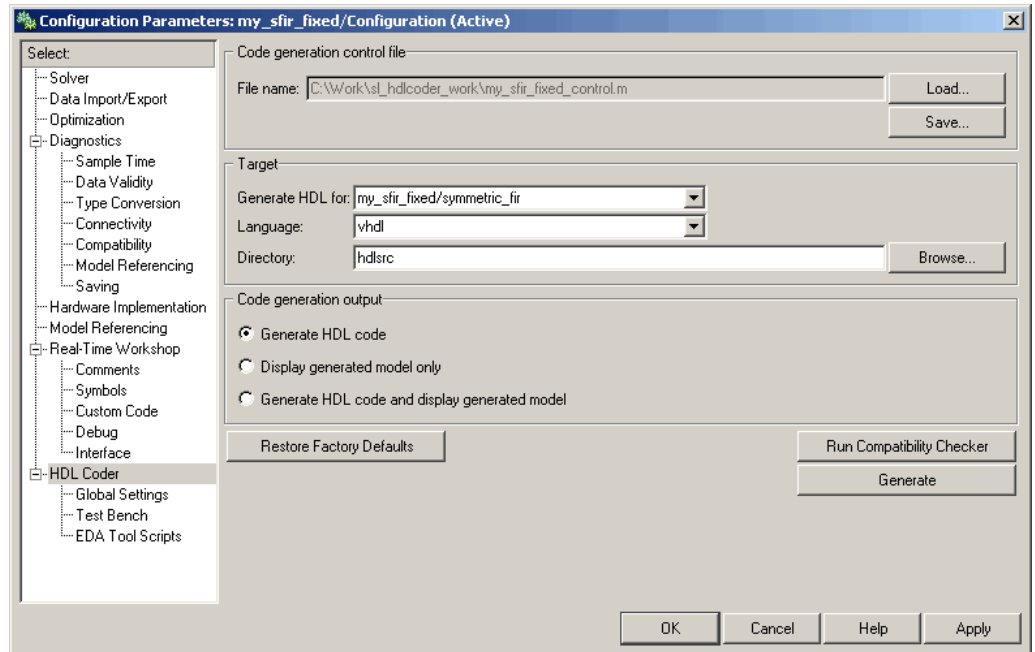
To save your current Simulink HDL Coder settings to a control file:

- 1 Open the Configuration Parameters dialog box and select the **HDL Coder** pane.
- 2 In the **Code generation control file** subpane, click **Save**.
- 3 If you have changed Simulink HDL Coder settings but have not yet applied them, the following prompt is displayed.



Click **Apply** to apply any Simulink HDL Coder option settings you may have changed.

- 4** A standard file dialog box opens. Navigate to the directory where you want to save the control file. This directory can be either the current working directory, or a directory that is in the MATLAB path. Do not locate the control file within the MATLAB directory tree, because it could be overwritten by subsequent MATLAB installations.
- 5** Enter the desired file name and save the file.
- 6** The control file name (with full absolute path and extension) is now displayed in the **File name** field, as shown in the following figure.



When the Simulink HDL Coder GUI saves or loads a control file, linkage between the model and the control file is established by an absolute path. If you want to load a control file using a relative path, use the `makehdl` or `makehdltb` functions, as described in “Associating an Existing Control File with Your Model” on page 5-19.

- 7 The control file is now linked to your model and is used when code is generated. Save the model if you want the control file linkage to persist in future MATLAB sessions with your model.

The control file you saved contains a `generateHDLFor` statement (see “`generateHDLFor`” on page 5-14) that specifies the Simulink path to the DUT specified in the **Generate HDL for** field. If you later select a different DUT for code generation, or make structural changes to your model (such as renaming the DUT), be sure to update this path information by resaving the control file.

The control file also preserves the values of all Simulink HDL Coder properties in the form of a call to the `set` method (see “set” on page 5-14). Properties are passed in to the call in alphabetical order.

- 8 If desired, you can now customize the control file using the MATLAB Editor or some other text editor. For example, you may want to add `ForEach` statements to define block implementation bindings. After you edit and save your changes to the control file, be sure to reload it by clicking **Load**.

### Creating a Control File Manually

You can create a control file manually using the MATLAB Editor or some other text editor. See “Structure of a Control File” on page 5-6 to make sure your files are set up correctly.

One reason for creating a control file manually is to create a control file that sets defaults for a subset of Simulink HDL Coder properties. See “Setting Up HDL Code Generation Defaults With a Control File” on page 5-22 for an example.

If you create a control file manually, you must link it to your model, as described in “Associating an Existing Control File with Your Model” on page 5-19

### Associating an Existing Control File with Your Model

A control file must be associated with your model before you can use the control file in code generation.

If you are generating code via `makehdl` or `makehdltb` from the MATLAB command prompt, use the `HDLControlFiles` property to specify the location of the control file. `HDLControlFiles` lets you specify either a full or relative path to the control file. In the following example, the control file is assumed to be located on the MATLAB path or in the current working directory, and to have the default file-name extension `.m`.

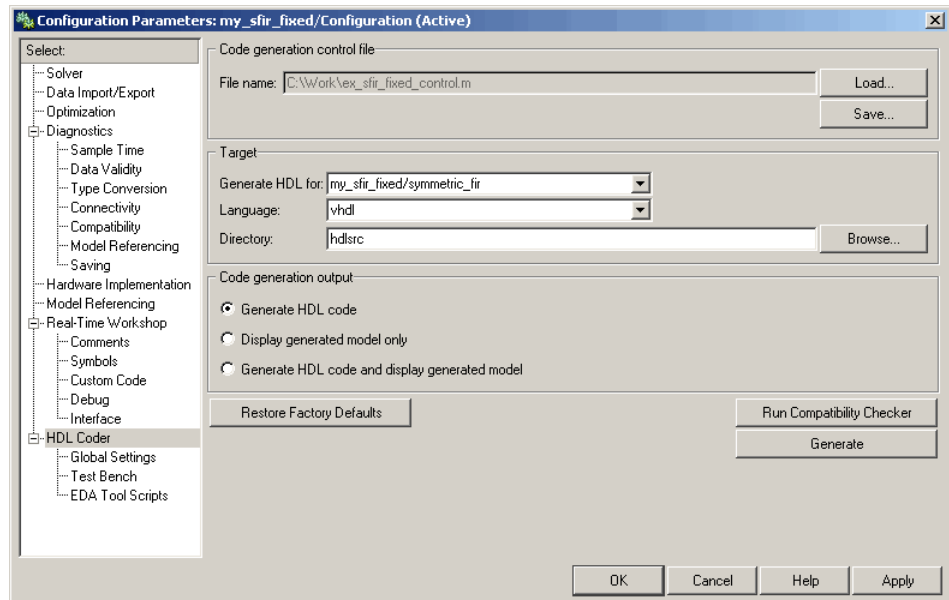
```
makehdl('HDLControlFiles', {'dct8config'});
```

If you are using the GUI to generate code, specify the location of the control file as follows:

- 1 Open the Configuration Parameters dialog box and select the **HDL Coder** pane.
- 2 Check the **File name** field to see if a control file is already linked to the model. If the **File name** field is blank, the model has no linked control file; proceed to step 3.

If the **File name** field is populated, the model is linked to a control file. If you want to replace that linkage and load in a different control file, proceed to step 3. Otherwise, no action is required.

- 3 In the **Code generation control file** subpane, click **Load**.
- 4 A standard file dialog box opens. Navigate to the desired control file and select it.
- 5 The control file name (with full absolute path and extension) appears in the **File name** field, as shown in the following figure.



- 6 Click **Apply**.



- 7** The control file is now linked to your model and is used when code is generated. Save the model if you want the control file linkage to persist in future MATLAB sessions with your model.

## Detaching a Control File from Your Model

The quickest (and recommended) way to detach a control file from your model is to click **Restore Factory Defaults**. This button removes the control file linkage, clears the **File name** field, and resets all Simulink HDL Coder properties to their default settings.

---

**Note Restore Factory Defaults** resets all HDL code generation settings. This action cannot be cancelled or undone. To recover previous settings, you must close the model without saving it, and then reopen it.

---

Any of the following actions also detach a control file from a model:

- Attach another control file, using either the **Load** button or a call to `makehdl`
- Close the model after attaching a control file, without saving the model
- Clear the `HDLControlFiles` property by passing a null file name argument to `makehdl`, as in this example:

```
makehdl(gcb, 'HDLControlFiles', {' '});
```

## Setting Up HDL Code Generation Defaults With a Control File

The Model Configuration Preferences dialog of the Model Explorer does not currently include Simulink HDL Coder settings. However, you can use a control file to define Simulink HDL Coder settings that you can subsequently load into any model. You can use such a control file to set up default or template HDL code generation settings for your projects or organization.

For example, suppose that you want the following settings to be applied to all models for a certain HDL project:

- Code is generated in Verilog.
- Generated code is written to a subdirectory of the user's working directory, named `vlog_gen_code`.
- Use of Verilog ``timescale` directives is disabled.

The following code example lists a control file that enforces these requirements:

```
function c = my_sfir_fixed_control

c = hdlnewcontrol(mfilename);
c.set( ...
    'TargetDirectory',      'vlog_gen_code',...
    'TargetLanguage',      'verilog',...
    'UseVerilogTimescale', 'off'...
);
```

An important feature of this control file is that it does not contain any code referencing elements that are specific to any particular model (such as Simulink paths in `generateHDLFor` or `forEach` calls). Therefore, the control file is portable and can be loaded into any model.

Loading a control file for the purpose of setting up defaults into a model is no different than loading any other control file (see “Associating an Existing Control File with Your Model” on page 5-19). However, if you load the same control file into multiple models, take care not to overwrite the original control file.

## Specifying Block Implementations and Parameters in the Control File

### In this section...

“Overview” on page 5-24

“Generating Selection/Action Statements with the `hdlnewforeach` Function” on page 5-25

“Blocks with Multiple Implementations” on page 5-29

### Overview

Simulink HDL Coder provides a default HDL block implementation for all supported blocks. In addition, Simulink HDL Coder provides selectable alternate HDL block implementations for several block types. Using selection/action statements (`forEach` or `forall` method calls) in a control file, you can specify the block implementation to be applied to all blocks of a given type (within a specific `modelscope`) during code generation. (See “Code Generation Control Objects and Methods” on page 5-8.) For many implementations, you can also pass in implementation parameters that provide additional control over code generation details.

You select HDL block implementations by specifying an implementation package and class, in the form `package.class`. Pass in the `package.class` specification and implementation parameters (if any) to the implementation argument of a `forEach` or `forall` call, as in the following example.

```
config.forEach('*', ...
    'built-in/Sum', {}, ...
    'hdldefaults.SumLinearHDL Emission', {'OutputPipeline', 2});
```

Given the `package.class` specification, Simulink HDL Coder will call the appropriate code generation method. You do not need to know any internal details of the implementation classes.

## Generating Selection/Action Statements with the `hdlnewforeach` Function

Determining the block path, type, implementation `package.class` specification, and implementation parameters for a large number of blocks in a model can be time-consuming. To help you create selection/action statements in your control files, Simulink HDL Coder provides the `hdlnewforeach` function. Given a selection of one or more blocks from your model, `hdlnewforeach` returns the following for each selected block, as string data in the MATLAB workspace:

- A `forEach` call coded with the correct `modelscope`, `blocktype`, and default implementation arguments for the block
- (Optional) A cell array of strings enumerating the available implementations for the block, in `package.class` form
- (Optional) A cell array of strings enumerating the names of implementation parameters (if any) corresponding to the block implementations. `hdlnewforeach` does not list data types and other details of block implementation parameters. These details are described in “Block Implementation Parameters” on page 5-47.

Having generated this information, you can copy and paste the strings into your control file.

### `hdlnewforeach` Example

This example uses `hdlnewforeach` to construct a `forEach` call that specifies generation of two pipeline stages after the output of a selected Sum block within the `sfir_fixed` demo model. To create the control file:

- 1 In the MATLAB window, select **File > New > M-File**. The MATLAB editor opens an empty M-file.
- 2 Create a skeletal control file by entering the following code into the M-file window:

```
function c = newforeachexamp
c = hdlnewcontrol(mfilename);

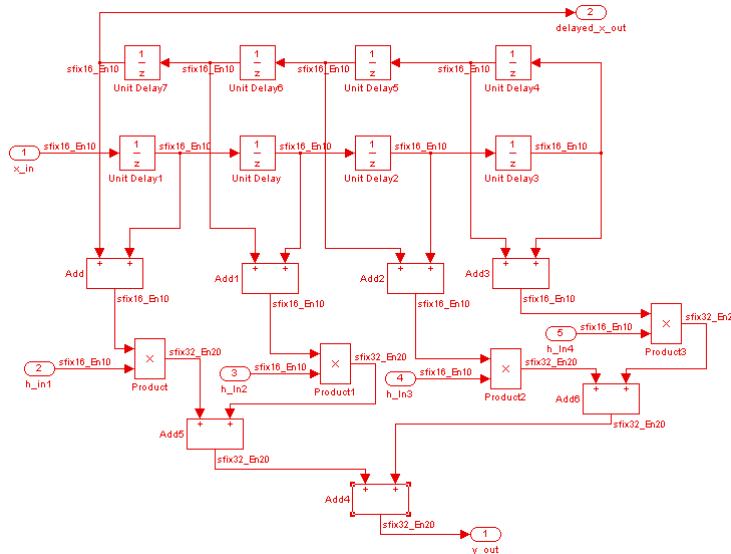
% Set top-level subsystem from which code is generated.
```

```
c.generateHDLFor('sfir_fixed/symmetric_fir');
% INSERT FOREACH CALL BELOW THIS LINE.
```

- 3** Save the file as newforeachexamp.m.
- 4** Open the sfir\_fixed demo model.
- 5** Before invoking hdlnewforeach, you must run checkhdl or makehdl to build in-memory information about the model. At the MATLAB command prompt, run checkhdl on the symmetric\_fir subsystem, as shown in the following code example:

```
checkhdl('sfir_fixed/symmetric_fir')
### Starting HDL Check.
### HDL Check Complete with 0 errors, warnings and messages.
```

- 6** Close the checkhdl report window and activate the sfir\_fixed model window.
- 7** In the symmetric\_fir subsystem window, select the Add4 block, as shown in the following figure.



Now you are ready to generate a `forEach` call for the selected block:

- 1 Type the following command at the MATLAB prompt.

```
[cmd,impl,parms] = hdlnewforeach(gcb)
```

- 2 The command returns the following results:

```
cmd =

c.forEach('sfir_fixed/symmetric_fir/Add4',...
'built-in/Sum', {},...
'hdldefaults.SumLinearHDLEmission', {});

impl =

{3x1 cell}

parms =

{1x1 cell}    {1x1 cell}    {1x1 cell}
```

The first return value, `cmd`, contains the generated `forEach` call. The `forEach` call specifies the default implementation for the Sum block: `hdldefaults.SumLinearHDLEmission`. Also by default, no parameters are passed in for this implementation.

- 3 The second return value, `impl`, is a cell array containing three strings representing the available implementations for the Sum block. The following example lists the contents of the `impl` array:

```
impl{1}

ans =

'hdldefaults.SumTreeHDLEmission'
'hdldefaults.SumLinearHDLEmission'
'hdldefaults.SumCascadeHDLEmission'
```

See the table “Built-In/Sum of Elements on page 5-33” for information about these implementations.

- 4** The third return value, `parms`, is a cell array containing three strings that represent the available implementations parameters corresponding to the previously listed Sum block implementations. The following example lists the contents of the `parms` array:

```
parms{1:3}

ans =

    'OutputPipeline'

ans =

    'OutputPipeline'

ans =

    'OutputPipeline'
```

This listing shows that each of the Sum block implementations has one parameter, 'OutputPipeline'. This indicates that a parameter/value pair of the form {'OutputPipeline',val} can be passed in with any of the Sum block implementations.

`hdlnewforeach` does not provide information about the data type, valid range, or other constraints on `val`. Some implementation parameters take numeric values, while others take strings. See “Block Implementation Parameters” on page 5-47 for details on implementation parameters.

- 5** Copy the three lines of `forEach` code from the MATLAB Command Window and paste them into the end of your `newforeachexamp.m` file:

```
% INSERT FOREACH CALL BELOW THIS LINE.
c.forEach('sfir_fixed/symmetric_fir/Add4',...
    'built-in/Sum', {},...
    'hdldefaults.SumLinearHDLEmission', {});
```



- 6** In this example, you will specify the default Sum block implementation for the Add4 block, but with generation of two pipeline stages before the final output. To do this, pass in the 'OutputPipeline' parameter with a value of 2. Modify the final line of the forEach call in your control file:

```
% INSERT FOREACH CALL BELOW THIS LINE.
c.forEach('sfir_fixed/symmetric_fir/Add4',...
'built-in/Sum', {},...
'hdldefaults.SumLinearHDL Emission', {'OutputPipeline', 2});
```

- 7** Save the control file.

- 8** The following code shows the complete control file:

```
function c = newforeachexamp
c = hdlnewcontrol(mfilename);

% Set top-level subsystem from which code is generated.
c.generateHDLFor('sfir_fixed/symmetric_fir');
% INSERT FOREACH CALLS HERE.
c.forEach('sfir_fixed/symmetric_fir/Add4',...
'built-in/Sum', {},...
'hdldefaults.SumLinearHDL Emission', {'OutputPipeline', 2});
```

The demo “Getting Started with Output Pipeline Commands in Control Files” gives a more detailed example of pipelining, including analysis of resulting clock rate improvements in a synthesized HDL model.

---

**Note** For convenience, `hdlnewforeach` supports a more abbreviated syntax than that used in the previous example. See the `hdlnewforeach` reference page.

---

## Blocks with Multiple Implementations

The tables in this section summarize the block types that have multiple implementations. The Implementations column gives the package.class

specification you should use in your control files. The Description column summarizes the trade-offs involved in choosing different implementations.

Simulink HDL Coder provides a default HDL block implementation for all supported blocks. If you want to use the default implementation, you do not usually need to specify it explicitly in a control file. However, the following example illustrates a situation in which the default implementation is specified as an exception for one particular block:

```
% 1. Use default (multipliers) Gain block implementation
% for one specific Gain block within OneD_DCT8 subsystem.
c.forEach('dct8_fixed/OneD_DCT8/Gain14',...
    'built-in/Gain', {},...
    'hdldefaults.GainMultHDL Emission');
% 2. Use factored CSD Gain block implementation
% or all other Gain blocks at or below
% level of OneD_DCT8 subsystem.
c.forEach('dct8_fixed/OneD_DCT8/*',...
    'built-in/Gain', {},...
    'hdldefaults.GainFCSDHDL Emission');
```

**Built-In/Gain**

Implementations	Description
hdldefaults.GainMultHDL Emission	<i>Default.</i> This implementation retains multiplier operations in HDL code generated by the Gain block.

**Built-In/Gain (Continued)**

Implementations	Description
<code>hdldefaults.GainCSDHDLEmission</code>	This implementation decreases the area used by the model while maintaining or increasing clock speed, using canonic signed digit (CSD) techniques. CSD replaces multiplier operations with shift and add operations. CSD minimizes the number of addition operations required for constant multiplication by representing binary numbers with a minimum count of nonzero digits.
<code>hdldefaults.GainFCSDHDLEmission</code>	This implementation lets you achieve a greater area reduction than CSD, at the cost of decreasing clock speed. This implementation uses factored CSD techniques, which replace multiplier operations with shift and add operations on prime factors of the operands.

**Built-In/Lookup Table**

Implementations	Description
<code>hdldefaults.LookupHDLEmission</code>	<i>Default.</i> Nonhierarchical lookup table.
<code>hdldefaults.LookupHDLInstantiation</code>	This implementation generates an additional level of HDL hierarchy (which does not exist in the Simulink model) for the lookup table.

**Signal Processing Blockset/Minimum**

Implementation	Description
<code>hdldefaults.MinMaxTreeHDLEmission</code>	<i>Default.</i> This implementation is large and slow but has minimal latency.
<code>hdldefaults.MinMaxCascadeHDLEmission</code>	This implementation is optimized for latency * area, with medium speed. See “A Note on Cascade Implementations” on page 5-34.

**Signal Processing Blockset/Maximum**

Implementation	Description
hdldefaults.MinMaxTreeHDLEmission	<i>Default.</i> This implementation is large and slow but has minimal latency.
hdldefaults.MinMaxCascadeHDLEmission	This implementation is optimized for latency * area, with medium speed. See “A Note on Cascade Implementations” on page 5-34.

**Built-In/MinMax**

Implementation	Description
hdldefaults.MinMaxTreeHDLEmission	<i>Default.</i> This implementation is large and slow but has minimal latency.
hdldefaults.MinMaxCascadeHDLEmission	This implementation is optimized for latency * area, with medium speed. See “A Note on Cascade Implementations” on page 5-34.

**Built-In/Product of Elements**

Implementation	Description
hdldefaults.ProductLinearHDLEmission	<i>Default.</i> Generates a chain of N operations (multipliers) for N inputs.
hdldefaults.ProductTreeHDLEmission	This implementation has minimal latency but is large and slow. It generates a tree-shaped structure of multipliers.
hdldefaults.ProductCascadeHDLEmission	This implementation optimizes latency * area and is faster than the tree implementation. It computes partial products and cascades multipliers. See “A Note on Cascade Implementations” on page 5-34.

**Built-In/Sum of Elements**

Implementation	Description
<code>hdldefaults.SumLinearHDLEmission</code>	<i>Default.</i> Generates a chain of N operations (adders ) for N inputs.
<code>hdldefaults.SumTreeHDLEmission</code>	This implementation has minimal latency but is large and slow. Generates a tree-shaped structure of adders.
<code>hdldefaults.SumCascadeHDLEmission</code>	This implementation optimizes latency * area and is faster than the tree implementation. It computes partial sums and cascades adders. See “A Note on Cascade Implementations” on page 5-34.

**Built-In/SubSystem**

Implementation	Description
<code>hdldefaults.SubsystemBlackBoxHDLInstantiation</code>	<p>This implementation generates a black box interface for subsystems. That is, the generated HDL code includes only the input/output port definitions for the subsystem. In this way, you can use a subsystem in your model to generate an interface to existing hand-written HDL code.</p> <p>The black box interface generated for subsystems is similar to the interface generated for Model blocks, but without generation of clock signals.</p>
<code>hdldefaults.NoHDLEmission</code>	This implementation completely removes the subsystem from the generated code. This lets you use a subsystem in simulation but treat it as a “no-op” in the HDL code.

For more information on subsystem implementations, see Chapter 8, “Interfacing Subsystems and Models to HDL Code”.

**Special-Purpose Implementations**

Implementation	Description
hdldefaults.PassThroughHDL Emission	Provides a pass-through implementation in which the block’s inputs are passed directly to its outputs. (In effect, the block becomes a wire in the HDL code.) Several blocks are supported with a pass-through implementation.
hdldefaults.NoHDL Emission	This implementation completely removes the block from the generated code. This lets you use the block in simulation but treat it as a “no-op” in the HDL code. This implementation is used for many blocks (such as Scopes and Assertions) that are significant in simulation but would be meaningless in HDL code. You can also use this implementation as an alternative implementation for subsystems.

For more information related to special-purpose implementations, see Chapter 8, “Interfacing Subsystems and Models to HDL Code”.

**A Note on Cascade Implementations**

Cascade implementations are available for the Sum of Elements, Product of Elements, and MinMax blocks. These implementations require multiple clock cycles to process their inputs; therefore, their inputs must be kept unchanged for their entire sample-time period. Simulink HDL Coder test benches accomplish this by using a register to drive the inputs.

A recommended design practice, when integrating HDL code generated by Simulink HDL Coder with other HDL code, is to provide registers at the inputs. While not strictly required, adding registers to the inputs improves timing and avoids problems with data stability for blocks that require multiple clock cycles to process their inputs.

## Summary of Block Implementations

The following table summarizes all blocks that are supported for HDL code generation and their available implementations in the current release. The columns signify

- *Simulink Block*: Library path and block name as displayed in Simulink.
- *Blockscope*: Block path and name to be passed as a blockscope string argument to `forEach` or `forAll`.
- *Implementations and Parameters*: Names of available implementations, and parameters supported for the implementation (if any).

When specifying an implementation argument to `forEach` or `forAll`, use the format `package.class`, for example, `hdldefaults.AssignmentHDL Emission` or `hdlstateflow.StateflowHDLInstantiation`. Almost all implementation classes currently belong to the package `hdldefaults`. In the following table, the package name is given explicitly only for classes that belong to some other package.

See “Block Implementation Parameters” on page 5-47 for information on implementation parameters and how to specify them.

Simulink Block	Blockscope	Implementations and Parameters
dsparch4/Digital Filter Note 1: When the Digital Filter block <b>Discrete-time filter object</b> option is selected, Filter Design HDL Coder is required to generate code for the block. Note 2: The Digital Filter block <b>Input port(s)</b> option is not supported for HDL code generation.	dsparch4/Digital Filter	DigitalFilterHDLInstantiation <i>Parameter:</i> OutputPipeline
dspindex/Multiport Selector	dspindex/Multiport Selector	MultiportSelectorHDL Emission <i>Parameter:</i> OutputPipeline

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
dspindex/Variable Selector	dspindex/Variable Selector	VariableSelectorHDLEmission <i>Parameter: OutputPipeline</i>
dspsigattribs/Convert 1-D to 2-D	dspsigattribs/Convert 1-D to 2-D	PassThroughHDLEmission <i>Parameter: OutputPipeline</i>
dspsigattribs/Frame Conversion	built-in/FrameConversion	FrameConversionHDLEmission <i>Parameter: OutputPipeline</i>
dspsigops/Delay	dspsigops/Delay	DSPDelayHDLEmission <i>Parameter: OutputPipeline</i>
dspsigops/Downsample	dspsigops/Downsample	DownsampleHDLEmission <i>Parameter: OutputPipeline</i>
dspsigops/Upsample	dspsigops/Upsample	UpsampleHDLEmission <i>Parameter: OutputPipeline</i>
dspsnks4/Matrix Viewer	dspsnks4/Matrix Viewer	NoHDLEmission
dspsnks4/Signal To Workspace	dspsnks4/Signal To Workspace	NoHDLEmission
dspsnks4/Spectrum Scope	dspsnks4/Spectrum Scope	NoHDLEmission
dspsnks4/Time Scope	built-in/Scope	NoHDLEmission
dspsnks4/Vector Scope	dspsnks4/Vector Scope	NoHDLEmission
dspsnks4/Waterfall	dspsnks4/Waterfall	NoHDLEmission
dspsrcs4/DSP Constant	dspsrcs4/DSP Constant	ConstantHDLEmission <i>Parameter: OutputPipeline</i>
dspstat3/Maximum	dspstat3/Maximum	MinMaxTreeHDLEmission MinMaxCascadeHDLEmission <i>Parameter: All implementations support OutputPipeline.</i>



<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
dspstat3/Minimum	dspstat3/Minimum	MinMaxTreeHDL Emission MinMaxCascadeHDL Emission <i>Parameter:</i> All implementations support OutputPipeline.
hdl demolib/Dual Port RAM	hdl demolib/Dual Port RAM	RamBlockDualHDL Instantiation <i>Parameter:</i> OutputPipeline
lfilelinklib/HDL Cosimulation	lfilelinklib/HDL Cosimulation	hdlincisive.IncisiveHDL Instantiation <i>Parameters:</i> See “Interface Generation Parameters” on page 5-48.
modelsimlib/HDL Cosimulation	modelsimlib/HDL Cosimulation	ModelSimHDL Instantiation <i>Parameters:</i> See “Interface Generation Parameters” on page 5-48.
modelsimlib/To VCD File	modelsimlib/To VCD File	NoHDL Emission
sflib/Chart	sflib/Chart	hdlstateflow .StateflowHDL Instantiation <i>Parameter:</i> OutputPipeline
simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled	simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled	UnitDelayEnabledHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Constant	built-in/Constant	ConstantHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Data Type Conversion	built-in/ DataTypeConversion	DataTypeConversionHDL Emission <i>Parameter:</i> OutputPipeline

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Commonly Used Blocks/Demux	built-in/Demux	DemuxHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Gain	built-in/Gain	GainMultHDLEmission GainFCSDHDLEmission GainCSDHDLEmission <i>Parameter:</i> All implementations support OutputPipeline.
simulink/Commonly Used Blocks/Ground	built-in/Ground	ConstantHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/In1	built-in/Inport	NoHDLEmission (Input ports are generated automatically.)
simulink/Commonly Used Blocks/Logical Operator	built-in/Logic	LogicHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Mux	built-in/Mux	MuxHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Out1	built-in/Outport	NoHDLEmission (Output ports are generated automatically.)

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Commonly Used Blocks/Product	built-in/Product	ProductLinearHDLEmission ProductTreeHDLEmission ProductCascadeHDLEmission <i>Parameter:</i> All implementations support OutputPipeline. <i>Note:</i> ProductTreeHDLEmission and ProductCascadeHDLEmission are supported for Product blocks having a single vector input that has two or more elements.
simulink/Commonly Used Blocks/Relational Operator	built-in/RelationalOperator	RelationalOperatorHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Scope	built-in/Scope	NoHDLEmission
simulink/Commonly Used Blocks/Sum	built-in/Sum	SumLinearHDLEmission SumTreeHDLEmission SumCascadeHDLEmission <i>Parameter:</i> All implementations support OutputPipeline. <i>Note:</i> SumTreeHDLEmission and SumCascadeHDLEmission are supported for Sum blocks having a single vector input that has two or more elements.
simulink/Commonly Used Blocks/Switch	built-in/Switch	SwitchHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Commonly Used Blocks/Terminator	built-in/Terminator	NoHDLEmission

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Commonly Used Blocks/Unit Delay	built-in/UnitDelay	UnitDelayHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Discrete/Integer Delay	simulink/Discrete/Integer Delay	IntegerDelayHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Discrete/Memory	built-in/Memory	MemoryHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Discrete/Tapped Delay	simulink/Discrete/Tapped Delay	TappedDelayHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Discrete/ Zero-Order Hold	built-in/ZeroOrderHold	ZeroOrderHoldHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Logic and Bit Operations/Bit Clear	simulink/Logic and Bit Operations/Bit Clear	BitOpsHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Logic and Bit Operations/Bit Set	simulink/Logic and Bit Operations/Bit Set	BitOpsHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Logic and Bit Operations/Bitwise Operator	simulink/Logic and Bit Operations/Bitwise Operator	BitOpsHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Logic and Bit Operations/Compare To Constant	simulink/Logic and Bit Operations/Compare To Constant	CompareToConstHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Logic and Bit Operations/Compare To Zero	simulink/Logic and Bit Operations/Compare To Zero	CompareToZeroHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Logic and Bit Operations/Shift Arithmetic	simulink/Logic and Bit Operations/Shift Arithmetic	BitOpsHDL Emission <i>Parameter:</i> OutputPipeline

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Lookup Tables/Lookup Table	built-in/Lookup	LookupHDLInstantiation LookupHDL Emission <i>Parameter:</i> All implementations support OutputPipeline.
simulink/Math Operations/Abs	built-in/Abs	AbsHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Math Operations/Add	built-in/Sum	SumTreeHDL Emission SumLinearHDL Emission SumCascadeHDL Emission <i>Parameter:</i> All implementations support OutputPipeline. <i>Note:</i> SumTreeHDL Emission and SumCascadeHDL Emission are supported for Add blocks having a single vector input that has two or more elements.
simulink/Math Operations/Assignment	built-in/Assignment	AssignmentHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Math Operations/Divide	built-in/Product	ProductCascadeHDL Emission ProductLinearHDL Emission ProductTreeHDL Emission <i>Parameter:</i> All implementations support OutputPipeline.

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Math Operations/Math Function (sqrt ) Note: Only the sqrt function is supported for HDL code generation. We recommend that you use the Math Function from the hdllib library, which has the sqrt selected in its <b>Function</b> menu.	built-in/Math	SqrtBitsetHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Math Operations/Matrix Concatenate	built-in/Concatenate	MuxHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Math Operations/MinMax	built-in/MinMax	MinMaxTreeHDL Emission MinMaxCascadeHDL Emission <i>Parameter:</i> All implementations support OutputPipeline.
simulink/Math Operations/Product of Elements	built-in/Product	ProductTreeHDL Emission ProductLinearHDL Emission ProductCascadeHDL Emission <i>Parameter:</i> All implementations support OutputPipeline.
simulink/Math Operations/Reshape	simulink/Math Operations/Reshape	PassThroughHDL Emission <i>Parameter:</i> OutputPipeline
simulink/Math Operations/Sign	built-in/Signum	SignumHDL Emission <i>Parameter:</i> OutputPipeline

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Math Operations/Subtract	built-in/Sum	SumTreeHDLEmission SumLinearHDLEmission SumCascadeHDLEmission <i>Parameter:</i> All implementations support OutputPipeline. <i>Note:</i> SumTreeHDLEmission and SumCascadeHDLEmission are supported for Subtract blocks having a single vector input that has two or more elements.
simulink/Math Operations/Sum of Elements	built-in/Sum	SumTreeHDLEmission SumLinearHDLEmission SumCascadeHDLEmission <i>Parameter:</i> All implementations support OutputPipeline. <i>Note:</i> SumTreeHDLEmission and SumCascadeHDLEmission are supported for Sum of Elements blocks having a single vector input that has two or more elements.
simulink/Math Operations/Unary Minus	simulink/Math Operations/Unary Minus	UnaryMinusHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Math Operations/Vector Concatenate	built-in/Concatenate	MuxHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Model Verification/Assertion	built-in/Assertion	NoHDLEmission
simulink/Model Verification/Check Discrete Gradient	simulink/Model Verification/Check Discrete Gradient	NoHDLEmission

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Model Verification/Check Dynamic Gap	simulink/Model Verification/Check Dynamic Gap	NoHDL Emission
simulink/Model Verification/Check Dynamic Lower Bound	simulink/Model Verification/Check Dynamic Lower Bound	NoHDL Emission
simulink/Model Verification/Check Dynamic Range	simulink/Model Verification/Check Dynamic Range	NoHDL Emission
simulink/Model Verification/Check Dynamic Upper Bound	simulink/Model Verification/Check Dynamic Upper Bound	NoHDL Emission
simulink/Model Verification/Check Input Resolution	simulink/Model Verification/Check Input Resolution	NoHDL Emission
simulink/Model Verification/Check Static Gap	simulink/Model Verification/Check Static Gap	NoHDL Emission
simulink/Model Verification/Check Static Lower Bound	simulink/Model Verification/Check Static Lower Bound	NoHDL Emission
simulink/Model Verification/Check Static Range	simulink/Model Verification/Check Static Range	NoHDL Emission
simulink/Model Verification/Check Static Upper Bound	simulink/Model Verification/Check Static Upper Bound	NoHDL Emission
simulink/Ports & Subsystems/Model	built-in/ModelReference	ModelReferenceHDLInstantiation <i>Parameters:</i> See “Interface Generation Parameters” on page 5-48.



<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Signal Attributes/Data Type Duplicate	simulink/Signal Attributes/Data Type Duplicate	NoHDLEmission
simulink/Signal Attributes/Data Type Propagation	simulink/Signal Attributes/Data Type Propagation	NoHDLEmission
simulink/Signal Attributes/Rate Transition	built-in/RateTransition	RateTransitionHDLEmission <i>Parameter: OutputPipeline</i>
simulink/Signal Attributes/Signal Conversion	built-in/SignalConversion	PassThroughHDLEmission <i>Parameter: OutputPipeline</i>
simulink/Signal Attributes/Signal Specification	built-in/ SignalSpecification	SignalSpecificationHDLEmission <i>Parameter: OutputPipeline</i>
simulink/Signal Routing/Index Vector	built-in/MultiPortSwitch	MultiPortSwitchHDLEmission <i>Parameter: OutputPipeline</i>
simulink/Signal Routing/Multiport Switch	built-in/MultiPortSwitch	MultiPortSwitchHDLEmission <i>Parameter: OutputPipeline</i>
simulink/Signal Routing/Selector	built-in/Selector	SelectorHDLEmission <i>Parameter: OutputPipeline</i>
simulink/Sinks/Display	built-in/Display	NoHDLEmission
simulink/Sinks/Floating Scope	built-in/Scope	NoHDLEmission
simulink/Sinks/Stop Simulation	built-in/Stop	NoHDLEmission
simulink/Sinks/To File	built-in/ToFile	NoHDLEmission
simulink/Sinks/To Workspace	built-in/ToWorkspace	NoHDLEmission
simulink/Sinks/XY Graph	simulink/Sinks/XY Graph	NoHDLEmission

<b>Simulink Block</b>	<b>Blockscope</b>	<b>Implementations and Parameters</b>
simulink/Sources/Counter Free-Running	simulink/Sources/Counter Free-Running	CounterFreeRunningHDLEmission <i>Parameter:</i> OutputPipeline
simulink/Sources/Counter Limited	simulink/Sources/Counter Limited	CounterLimitedHDLEmission <i>Parameter:</i> OutputPipeline
simulink/User-Defined Functions/Embedded MATLAB Function	simulink/User-Defined Functions/Embedded MATLAB Function	hdlstateflow .StateflowHDLInstantiation <i>Parameter:</i> OutputPipeline

## Block Implementation Parameters

### In this section...

“Overview” on page 5-47

“OutputPipeline” on page 5-47

“Interface Generation Parameters” on page 5-48

### Overview

Block implementation parameters let you control details of the code generated for specific block implementations. Block implementation parameters are passed to `forEach` or `forall` calls (see “`forEach`” on page 5-8) as cell arrays of property/value pairs of the form

```
{'PropertyName', value}
```

Property names are strings. The data type of a property value is specific to the property. This section describes the syntax of each block implementation parameter, and how the parameter affects generated code.

### OutputPipeline

`OutputPipeline` lets you specify a pipelined implementation for selected blocks. The parameter value specifies the number of pipeline stages ( pipeline depth) in the generated code.

Syntax:

```
{'OutputPipeline', nStages}
```

where `nStages >= 0`.

The following `forEach` call specifies a pipeline depth of two stages for all `Sum` blocks in the model:

```
config.forEach('*',...  
    'built-in/Sum', {},...  
    'hdldefaults.SumLinearHDLEmission', {'OutputPipeline', 2});
```

### **Interface Generation Parameters**

Some block implementation parameters let you customize features of an interface generated for the following block types:

- simulink/Ports & Subsystems/Model
- built-in/Subsystem
- lfilinklib/HDL Cosimulation
- modelsimlib/HDL Cosimulation

For example, you can specify generation of a black box interface for a subsystem, and pass parameters that specify the generation and naming of clock, reset, and other ports in HDL code. For more information about interface generation parameters, see “Customizing the Generated Interface” on page 8-12.

## Restrictions on Use of Blocks in the Test Bench

In a Simulink model intended for use in HDL code generation, the DUT is typically modeled as a subsystem at the top level of the model, driven by other blocks or subsystems at the top level. These components make up the test bench.

Blocks that belong to the blocksets and toolboxes in the following list should not be directly connected to the DUT at the top level of the model. Instead, they should be placed in a subsystem, which is then connected to the DUT. All blocks in the following blocksets are subject to this restriction:

- RF Blockset
- SimDriveLine
- SimEvents
- SimMechanics
- SimPowerSystems
- Simscape



# Generating Bit-True Cycle-Accurate Models

---

Overview of Generated Models  
(p. 6-2)

Motivation for generating bit-true and cycle-accurate models; summary of model generation features

Example: Numeric Differences  
(p. 6-4)

Model generation case study illustrating numeric differences between original and generated models

Example: Latency (p. 6-8)

Model generation case study illustrating latency introduced in HDL code and generated model

Defaults and Options for Generated Models (p. 6-12)

Defaults used in model generation; GUI options and makehdl properties related to generated models

Fixed-Point and Double Precision Limitations for Generated Models (p. 6-17)

Describes how HDL code results may differ from generated model results in cases where Simulink fixed-point word size or double precision limits are exceeded

## Overview of Generated Models

In some circumstances, significant differences in behavior can arise between a Simulink model and the HDL code generated from that model. Such differences fall into two categories:

- *Numerics*: differences in intermediate and/or final computations. For example, a selected block implementation may restructure arithmetic operations to optimize for speed (see “Example: Numeric Differences” on page 6-4). Where such numeric differences exist, the HDL code is no longer *bit-true* to the Simulink model.
- *Latency*: insertion of delays of one or more clock cycles at certain points in the HDL code. Some block implementations that optimize for area can introduce these delays. Where such latency exists, the timing of the HDL code is no longer *cycle-accurate* with respect to the Simulink model.

To help you evaluate such cases, Simulink HDL Coder creates a *generated model* that is bit-true and cycle-accurate with respect to the generated HDL code. The generated model lets you

- Run Simulink simulations that accurately reflect the behavior of the generated HDL code.
- Create test benches based on the generated model, rather than the original model.
- Visually detect (by color highlighting of affected subsystems) all differences between the original and generated models.

Simulink HDL Coder always creates a generated model as part of the code generation process, and always generates test benches based on the generated model, rather than the original model. In cases where no latency or numeric differences occur, you can disregard the generated model except when generating test benches.

Simulink HDL Coder also provides options that let you

- Suppress display of the generated model.
- Create and display the only generated model, with code generation suppressed.



- Specify the color highlighting of differences between the original and generated models.
- Specify a name or prefix for the generated model.

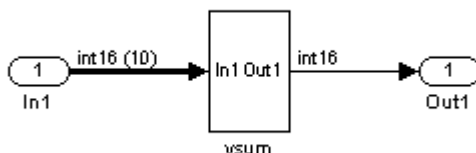
These options are described in “Defaults and Options for Generated Models” on page 6-12.

## Example: Numeric Differences

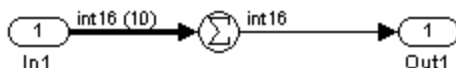
This example first examines a simple model that uses a code generation control file to select a speed-optimized Sum block implementation. It then examines a generated model and locates the numeric changes introduced by the optimization.

If you are not familiar with code generation control files and selection of block implementations, see Chapter 5, “Code Generation Control Files”.

The model, `simplevectorsum`, consists of a subsystem, `vsum`, driven by a vector input of width 10, with a scalar output. The following figure shows the root level of the model.



The device under test is the `vsum` subsystem, shown in the following figure. The subsystem contains a Sum block, configured for vector summation.



The model is configured to use a code generation control file, `svsumctrl.m`. The control file (shown in the following listing) maps the `SumTreeHDL Emission` implementation to the Sum block within the `vsum` subsystem. This implementation, optimized for minimal latency, generates a tree-shaped structure of adders for the Sum block.

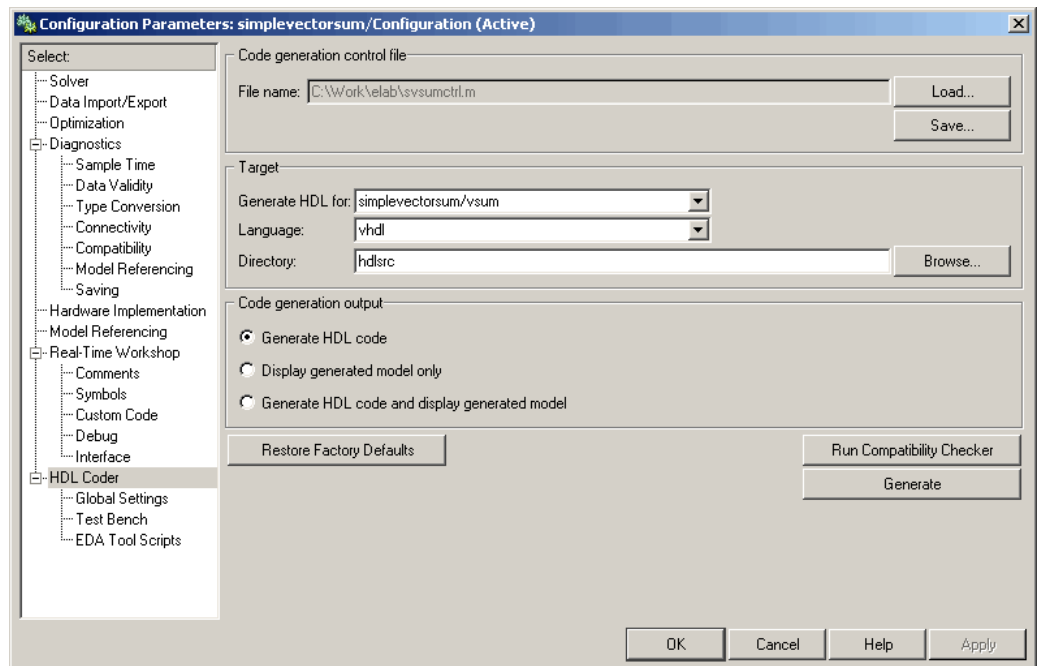
```
function config = svsumctrl
% Code generation control file for simplevectorsum model.
```

```

config = hdlnewcontrol(mfilename);
% Specify tree-structured adders implementaton for Sum block.
config.forEach('simplevectorsum/vsum/Sum',...
    'built-in/Sum',{},...
    'hdldefaults.SumTreeHDL Emission',{ });

```

The **File name** field of the Configuration Parameters dialog box (shown in the following figure) specifies that this control file is to be used during code generation.



When code generation is initiated, Simulink HDL Coder displays messages similar to those shown in the following example. The messages indicate that the control file is applied; control file processing is followed by creation of the generated model and generation of HDL code.

```

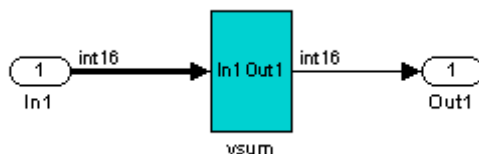
### Applying HDL Code Generation Control Statements
### 1 Control Statements to be applied

```

```
### Begin Model Generation
### Generating new model: gm_simplevectorsum.mdl
### Model Generation Complete.

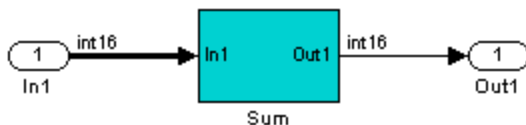
### Begin VHDL Code Generation
### Generating package file hdlsrc\vsum_pkg.vhd
### Working on simplevectorsum/vsum as hdlsrc\vsum.vhd
### HDL Code Generation Complete.
```

The generated model, gm\_ simplevectorsum, is displayed after code generation. This model is shown in the following figure.

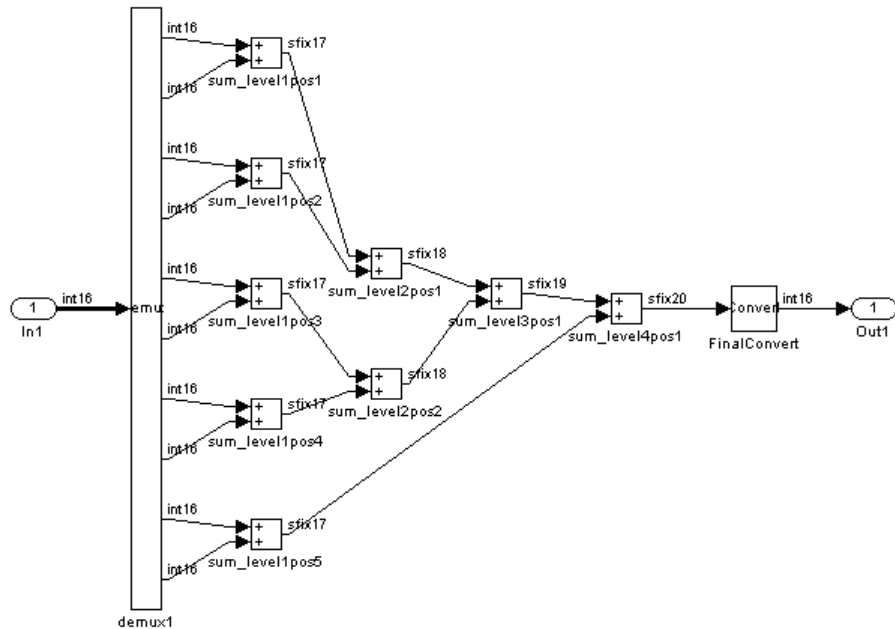


At the root level, this model appears identical to the original model, except that the vsum subsystem has been highlighted in cyan. This highlighting indicates that the subsystem differs in some respect from the vsum subsystem of the original model.

The following figure shows the vsum subsystem in the generated model. Observe that the Sum block is now implemented as a subsystem, which is also highlighted.



The following figure shows the internal structure of the Sum subsystem.



The vector sum is implemented as a tree of adders (Sum blocks). The vector input signal is demultiplexed and connected, as five pairs of operands, to the five leftmost adders. The widths of the adder outputs increase from left to right, as required to avoid overflow in computing intermediate results. A Data Conversion block, inserted before the final output, converts the 20-bit fixed-point result to the int16 data type required by the model.

## Example: Latency

This example uses the `simplevectorsum_cascade` model. This model is identical to the model in the previous example (“Example: Numeric Differences” on page 6-4), except that it uses a control file that selects a cascaded implementation for the Sum block. This implementation introduces both latency and numeric differences.

The model is configured to use the control file `svsum_cascade_ctrl.m`. The control file (shown in the following listing) maps the `SumCascadeHDL Emission` implementation to the Sum block within the `vsum` subsystem. This implementation generates a cascade of adders for the Sum block.

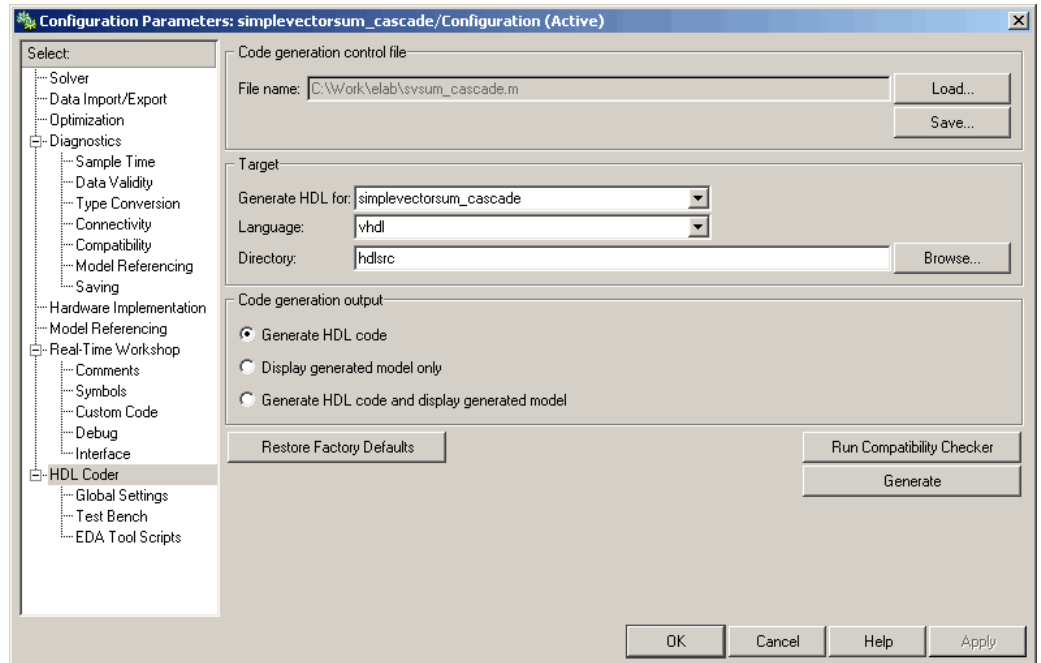
```
function config = svsum_cascade_ctrl
% Code generation control file for simplevectorsum model.

config = hdlnewconfig(mfilename);

% specify cascaded adders implementation for Sum block

config.forEach('simplevectorsum_cascade/vsum/Sum',...
    'built-in/Sum',{},...
    'hdldefaults.SumCascadeHDL Emission',{});
```

The **File name** field of the Configuration Parameters dialog box (shown in the following figure) specifies that this control file is used during code generation.



When code generation is initiated, Simulink HDL Coder displays messages similar to those shown in the following example. The messages indicate that the control file is applied; control file processing is followed by creation of the generated model and generation of HDL code.

```

### Applying HDL Code Generation Control Statements
###   1 Control Statements to be applied

### Begin Model Generation
### Generating new model: gm_simplevectorsum_cascade.mdl
### Model Generation Complete.

### Begin VHDL Code Generation
### Generating package file hdlsrc\simplevectorsum_cascade_pkg.vhd
### Working on simplevectorsum_cascade/vsum as hdlsrc\vsum.vhd
### Working on Timing Controller as hdlsrc\Timing_Controller.vhd
### Working on simplevectorsum_cascade as hdlsrc\simplevectorsum_cascade.vhd
### HDL Code Generation Complete.

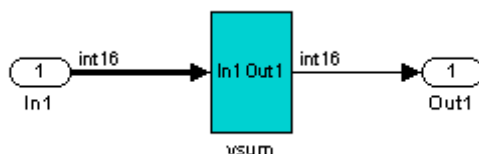
```

In the generated code, partial sums are computed by adders arranged in a cascade structure. Each adder computes a partial sum by demultiplexing and adding several inputs in succession. These computation take several clock cycles. On each cycle, an addition is performed; the result is then added to the next input.

To complete all computations within one sample period, the system master clock runs faster than the nominal sample rate of the system. A latency of one clock cycle (in the case of this model) is required to transmit the final result to the output. The inputs cannot change until all computations have been performed and the final result is presented at the output.

The generated HDL code runs at two effective rates: a faster rate for internal computations, and a slower rate for input/output. A special `Timing_Controller` entity generates these rates from a single master clock using counters and multiple clock enables. The `Timing_Controller` entity definition is written to a separate code file.

The generated model, `gm_simplevectorsum_cascade`, is displayed after code generation. This model is shown in the following figure.

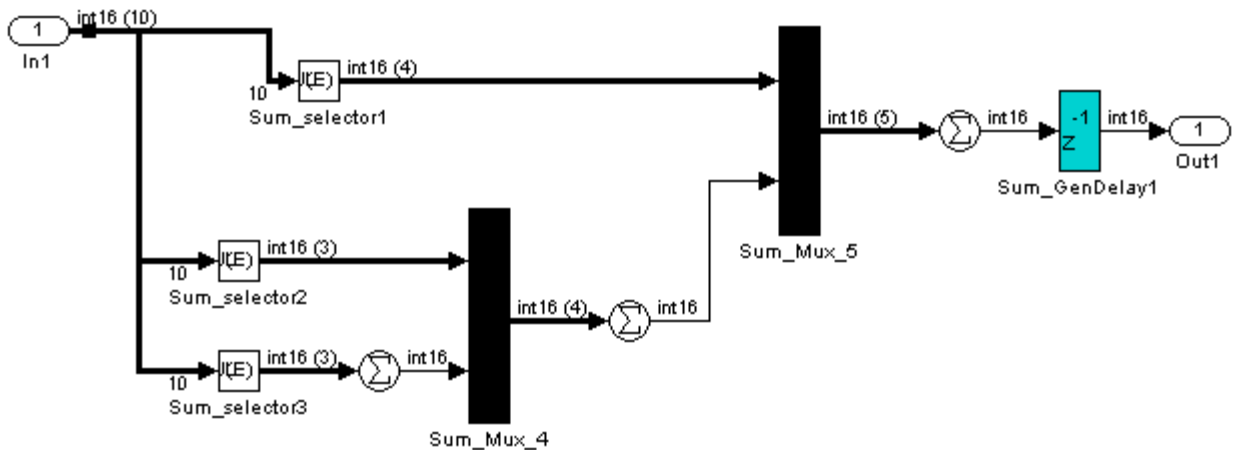


As in the previous (`gm_simplevectorsum`) example, the `vsum` subsystem is highlighted in cyan. This highlighting indicates that the subsystem differs in some respect from the `vsum` subsystem of the original model.

The following block diagram shows the `vsum` subsystem in the generated model. The subsystem has been restructured to reflect the structure of the generated HDL code; inputs are grouped and routed to three adders for partial sum computations.



A Unit Delay (highlighted in cyan) has been inserted before the final output. This block delays, (in this case for one sample period), the appearance of the final sum at the output. The delay reflects the latency of the generated HDL code.



**Note** The HDL code generated from the example model used in this section is bit-true to the original Simulink model.

However, in some cases, cascaded block implementations can produce numeric differences between the original Simulink model and the generated HDL code, in addition to the introduction of latency. Numeric differences can arise from saturation and rounding operations.

## Defaults and Options for Generated Models

In this section...
“Defaults for Model Generation” on page 6-12
“GUI Options” on page 6-13
“Generated Model Properties for makehdl” on page 6-14

### Defaults for Model Generation

This section summarizes the defaults used by Simulink HDL Coder when generated models are built.

#### Model Generation

Simulink HDL Coder always creates a generated model as part of the code generation process. The generated model is built in memory, before actual generation of HDL code. The HDL code and the generated model are bit-true and cycle-accurate with respect to one another.

---

**Note** The in-memory generated model is not written to a model file unless you explicitly save it.

---

#### Naming of Generated Models

The naming convention for generated models is

`prefix_modelname`

where the default prefix is `gm_`, and the default `modelname` is the name of the original model.

If code is generated more than once from the same original model, and previously generated model(s) exist in memory, an integer is suffixed to the name of each successively generated model. The suffix ensures that each generated model has a unique name. For example, if the original model is

named test, generated models will be named gm\_test, gm\_test0, gm\_test1, etc.

---

**Note** Take care, when regenerating code from your models, to select the original model for code generation, not a previously generated model. Generating code from a generated model may introduce unintended delays or numeric differences that could make the model operate incorrectly.

---

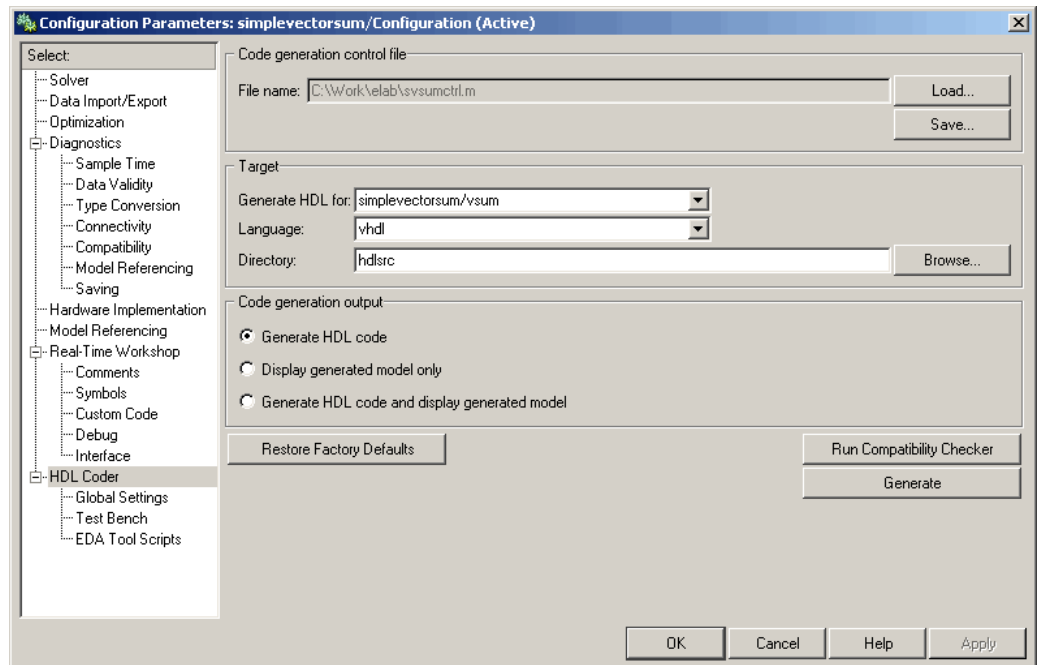
## Block Highlighting

By default, blocks in a generated model that differ from the original model, and their ancestor (parent) blocks in the model hierarchy, are highlighted in the default color, cyan. You can quickly see whether any differences have been introduced, by examining the root level of the generated model.

If there are no differences between the original and generated models, no blocks will be highlighted.

## GUI Options

The Simulink HDL Coder GUI provides high-level options controlling the generation and display of generated models. More detailed control is available through the makehdl command (see “Generated Model Properties for makehdl” on page 6-14). Generated model options are located in the top-level **HDL Options** pane of the Configuration Parameters dialog box, as shown in the following figure.



The options are

- **Generate HDL code:** (Default) Generate code, but do not display the generated model.
- **Display generated model only:** Create and display the generated model, but do not proceed to code generation.
- **Generate HDL code and display generated model:** Generate both code and model, and display the model when completed.

### Generated Model Properties for makehdl

The following table summarizes makehdl properties that provide detailed controls for the generated model.

<b>Property and Value(s)</b>	<b>Description</b>
'GeneratedmodelNameprefix', ['string']	The default name for the generated model is gm_modelname, where gm_ is the default prefix and modelname is the original model name. To override the default prefix, assign a string value to this property.
'Generatemodelname', ['string']	By default, the original model name is used as the modelname substring of the generated model name. To specify a different model name, assign a string value to this property.
'CodeGenerationOutput', 'string'	Controls the production of generated code and display of the generated model. Values are <ul style="list-style-type: none"><li>• GenerateHDLCode: (Default) Generate code, but do not display the generated model.</li><li>• GenerateHDLCodeAndDisplayGeneratedModel: Create and display generated model, but do not proceed to code generation.</li><li>• DisplayGeneratedModelOnly: Generate both code and model, and display model when completed.</li></ul>

<b>Property and Value(s)</b>	<b>Description</b>
'Highlightancestors', ['on'   'off']	By default, blocks in a generated model that differ from the original model, and their ancestor (parent) blocks in the model hierarchy, are highlighted in a color specified by the Highlightcolor property. If you do not want the ancestor blocks to be highlighted, set this property to 'off'.
'Highlightcolor', 'RGBName'	Specify the color used to highlight blocks in a generated model that differ from the original model (default: cyan). Specify the color (RGBName) as one of the following color string values: <ul style="list-style-type: none"><li>• cyan (default)</li><li>• yellow</li><li>• magenta</li><li>• red</li><li>• green</li><li>• blue</li><li>• white</li><li>• black</li></ul>

# Fixed-Point and Double Precision Limitations for Generated Models

## In this section...

“Fixed-Point Limitation” on page 6-17

“Double Precision Limitation” on page 6-17

## Fixed-Point Limitation

The maximum fixed-point word size in Simulink is 128 bits. HDL does not have such a limit. This can lead to cases in which the generated HDL code is not bit-true to the generated model.

When the result of a computation in the generated HDL code has a word size greater than 128 bits:

- Simulink HDL Coder issues a warning.
- Computations in the generated model (and the generated HDL test bench) are limited to a result word size of 128 bits.
- This word size limitation does not apply to the generated HDL code, so results returned from the HDL code may not match the HDL test bench or the generated model.

## Double Precision Limitation

When the binary point in double-precision computations is very large or very small, the scaling can become `inf` or `0`. The limits of precision in MATLAB can be expressed as follows:

```
log2(realmin) ==> -1022
```

```
log2(realmax) ==> 1024
```

Where these limits are exceeded, the binary point is saturated and a warning is issued. If the generated HDL code has binary point scaling greater than  $2^{1024}$ , the generated model has a maximum scaling of  $2^{1024}$ .

Similarly if the generated HDL code has binary point scaling smaller than  $2^{-1022}$ , then the generated model has scaling of  $2^{-1022}$ .



# HDL Compatibility, Code Tracing, and Block Support Reports

---

HDL Compatibility Checker (p. 7-2)	How to check your models for HDL code generation compatibility
Code Tracing Using the Mapping File (p. 7-6)	How to use a mapping file to trace generated HDL entities back to the corresponding Simulink systems
Supported Blocks Library (p. 7-9)	How to create a library of all blocks that are currently supported for HDL code generation

## HDL Compatibility Checker

The HDL compatibility checker lets you check whether a subsystem or model is compatible with HDL code generation. You can run the compatibility checker from the MATLAB command line or an M-file script, or from the Simulink GUI.

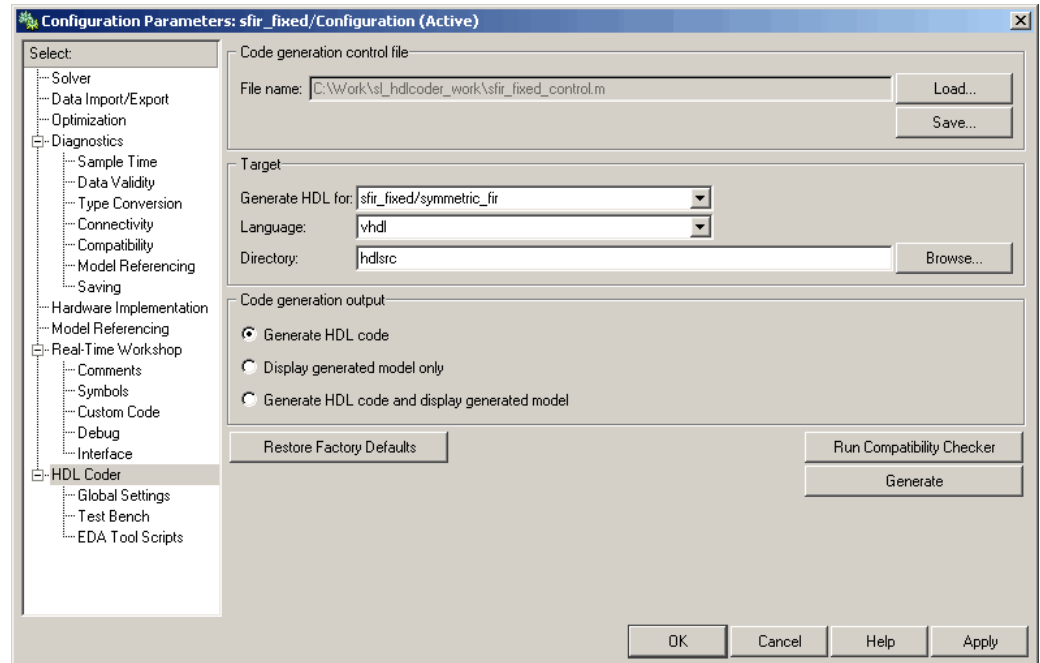
To run the compatibility checker from the command line or an M-file script, use the `checkhdl` function. The syntax of the function is

```
checkhdl('system')
```

where *system* is the device under test (DUT), typically a subsystem within the current Simulink model.

To run the compatibility checker from the Simulink GUI:

- 1 Open the Configuration Parameters dialog box or the Model Explorer. Select the **HDL Coder** options category. The following figure shows the **HDL Coder** pane of the Configuration Parameters dialog box.



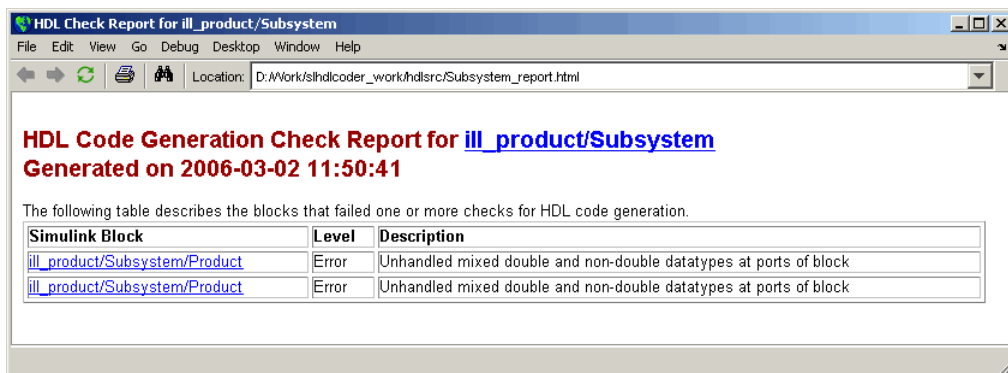
**2** Select the subsystem you want to check from the **Generate HDL for** pop-up menu.

**3** Click the **Run Compatibility Checker** button.

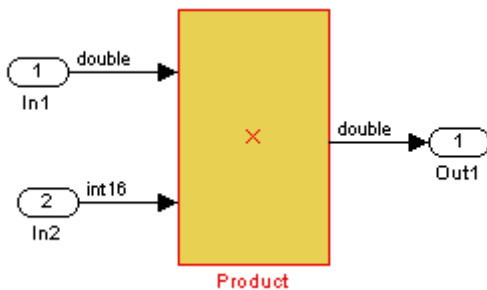
The HDL compatibility checker examines the specified system for any compatibility problems, such as use of unsupported blocks, illegal data type usage, etc. The HDL compatibility checker generates an HDL Code Generation Check Report, which is stored in the target directory. The report file naming convention is *system\_report.html*, where *system* is the name of the subsystem or model that was passed in to the HDL compatibility checker.

The HDL Code Generation Check Report is displayed in a browser window. Each entry in the HDL Code Generation Check Report is hyperlinked to the block or subsystem that caused the problem. When you click the hyperlink, Simulink highlights and displays the block of interest (provided that the model referenced by the report is open).

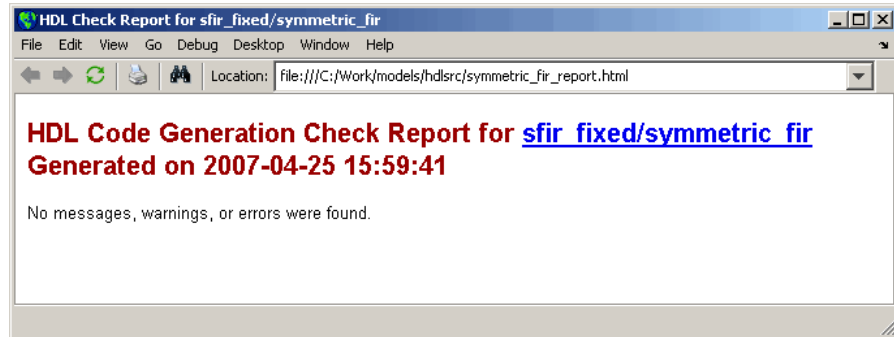
The following figure shows an HDL Code Generation Check Report that was generated for a subsystem with a Product block that was configured with a mixture of double and integer port data types. This configuration is legal in Simulink, but incompatible with Simulink HDL Coder.



When you click the hyperlink in the left column, Simulink opens the subsystem containing the offending block. The block of interest is highlighted, as shown in the following figure.



The following figure shows an HDL Code Generation Check Report that was generated for a subsystem that passed all compatibility checks. In this case, the report contains only a hyperlink to the subsystem that was checked.



## Code Tracing Using the Mapping File

---

**Note** This section refers to generated VHDL entities or Verilog modules generically as “entities.”

---

A *mapping file* is a text report file generated by `makehdl`. Mapping files are generated as an aid in tracing generated HDL entities back to the corresponding Simulink systems.

A mapping file shows the relationship between systems in the Simulink model and the VHDL entities or Verilog modules that were generated from them. A mapping file entry has the form

```
Simulink_path --> HDL_name
```

where *Simulink\_path* is the full Simulink path to a system in the Simulink model and *HDL\_name* is the name of the VHDL entity or Verilog module that was generated from that system. The mapping file contains one entry per line.

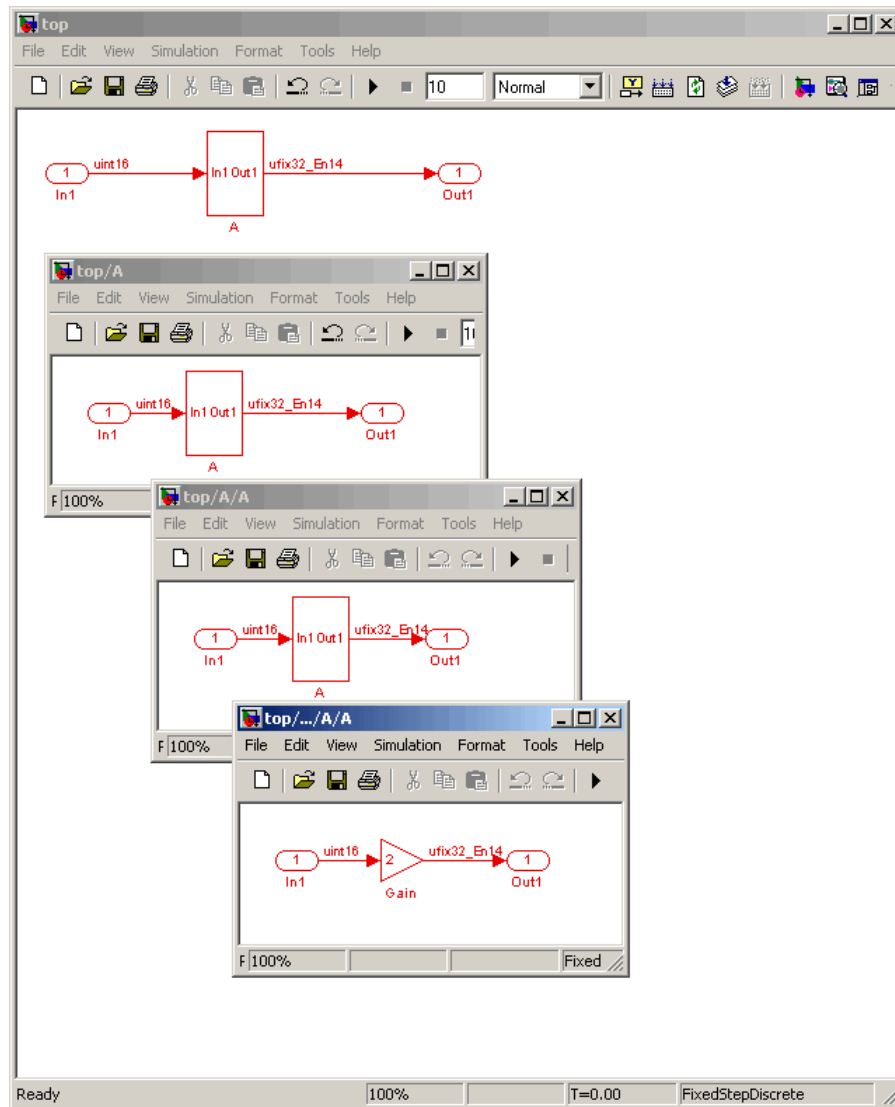
In simple cases, the mapping file may contain only one entry. For example, the `symmetric_fir` subsystem of the `sfir_fixed` demo model generates the following mapping file:

```
sfir_fixed/symmetric_fir --> symmetric_fir
```

Mapping files are more useful when HDL code is generated from complex models where multiple subsystems generate many entities, and in cases where conflicts between identically named subsystems are resolved by Simulink HDL Coder.

If a subsystem name is unique within the model, Simulink HDL Coder simply uses the subsystem name as the generated entity name. Where identically named subsystems are encountered, Simulink HDL Coder attempts to resolve the conflict by appending a postfix string (by default, `'_entity'`) to the conflicting subsystem. If subsequently generated entity names conflict in turn with this name, incremental numerals (1, 2, 3, . . . *n*) are appended.

As an example, consider the model shown in the following figure. The top-level model contains subsystems named A nested to three levels.



When code is generated for the top-level subsystem A, makehdl works its way up from the deepest level of the model hierarchy, generating unique entity names for each subsystem.

```
makehdl('top/A')
### Working on top/A/A/A as A_entity1.vhd
### Working on top/A/A as A_entity2.vhd
### Working on top/A as A.vhd

### HDL Code Generation Complete.
```

The following example lists the contents of the resultant mapping file.

```
top/A/A/A --> A_entity1
top/A/A --> A_entity2
top/A --> A
```

Given this information, you could trace any generated entity back to its corresponding subsystem by using the `open_system` command, for example:

```
open_system('top/A/A')
```

Each generated entity file also contains the Simulink path for its corresponding subsystem in the header comments at the top of the file, as in the following code excerpt.

```
-- Module: A_entity2
-- Simulink Path: top/A
-- Created: 2005-04-20 10:23:46
-- Hierarchy Level: 0
```



## Supported Blocks Library

Simulink HDL Coder provides an M-file utility, `hdl1lib.m`, that creates a library of all blocks that are currently supported for HDL code generation.

The block library, `hdl1supported.mdl`, affords quick access to all supported blocks. By constructing models using blocks from this library, you can ensure compatibility with Simulink HDL Coder.

The set of supported blocks will change in future releases of Simulink HDL Coder. To keep the `hdl1supported.mdl` current, The MathWorks recommends that you rebuild the library each time you install a new release. To create the library:

- 1 Type the following at the MATLAB prompt:

```
hdl1lib
```

`hdl1lib` starts generation of the `hdl1supported` library. Simulink loads many libraries during the creation of the `hdl1supported` library. When `hdl1lib` completes generation of the library, it does not unload these libraries.

- 2 After the library is generated, you must save it to a directory of your choice. You should retain the file name `hdl1supported.mdl`, because this document refers to the supported blocks library by that name.



# Interfacing Subsystems and Models to HDL Code

---

Overview of HDL Interfaces (p. 8-2)	Overview of HDL interfaces generated by Simulink HDL Coder
Generating a Black Box Interface for a Subsystem (p. 8-3)	How to generate an interface to existing or legacy HDL code from a subsystem
Generating Interfaces for Referenced Models (p. 8-6)	Code generation for models referenced within a Model block
Code Generation for HDL Cosimulation Blocks (p. 8-7)	Generating an interface to HDL code for cosimulation with HDL simulators
Generating an Interface for the Dual Port RAM Block (p. 8-9)	Code generation for the Dual Port RAM block
Customizing the Generated Interface (p. 8-12)	How to use block implementation parameters to control generation and naming of ports and other attributes of the generated interface
Pass-Through and No-Op Implementations (p. 8-14)	Bypassing or omitting selected subsystems in generated code
Limitation on Generated Verilog Interfaces (p. 8-15)	Describes a limitation in the current release that applies to generation of Verilog interfaces for some blocks

### Overview of HDL Interfaces

Simulink HDL Coder provides a number of different ways to generate interfaces to your hand-written or legacy HDL code. Depending on your application, you may want to generate such an interface from different levels of your model:

- Subsystem
- Model referenced by a higher-level model
- Cosimulation block
- Dual Port RAM block

For most such interfaces, you can use interface generation parameters in your control file to control generation and naming of ports and other attributes of the generated interface.

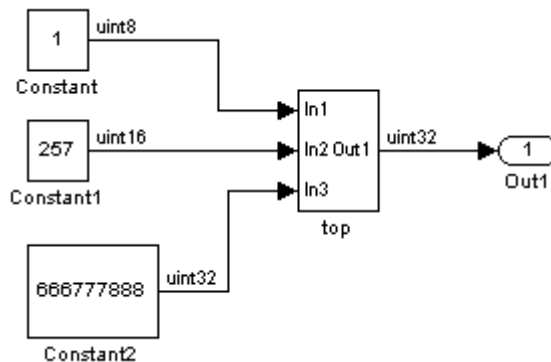
You can also generate a pass-through (wire) HDL implementation for a subsystem, or omit code generation entirely for a subsystem. Both of these techniques can be useful in cases where you need a subsystem in your simulation, but do not need the subsystem in your generated HDL code.

## Generating a Black Box Interface for a Subsystem

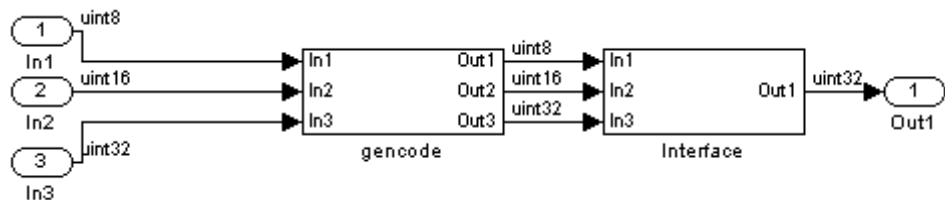
A *black box* interface for a subsystem is a generated VHDL component or Verilog module that includes only the HDL input/output port definitions for the subsystem. By generating such a component, you can use a subsystem in your model to generate an interface to existing hand-written HDL code.

To generate the interface, you use a control file to map one or more Subsystem blocks to the `hdldefaults.SubsystemBlackBoxHDLInstantiation` implementation. (See Chapter 5, “Code Generation Control Files” for a detailed description of the structure and use of control files.)

As an example, consider the model and subsystem shown in the following figures. The model, `subsysstst`, contains a subsystem, `top`, which is the device under test.



The subsystem `top` contains two lower-level subsystems, `gencode` and `Interface`.



Suppose that you want to generate HDL code from top, with a black box interface from the Interface subsystem. The first step would be to create a control file that defines the Simulink path and block type for the Interface subsystem, and maps this subsystem to the `hdldefaults.SubsystemBlackBoxHDLInstantiation` implementation. The following listing shows an example control file.

```
% Code generation control file - blackbox_ctrl.m
function control = blackbox_ctrl
control = hdlnewcontrol(mfilename);
% Generate a black box interface for the subsystem labeled
% Interface within the top-level device

control.forEach( ...
    'subsystst/top/Interface', ...
    'built-in/SubSystem', {}, ...
    'hdldefaults.SubsystemBlackBoxHDLInstantiation');
```

The control file is attached to the model when code generation is invoked. In the following `makehdl` command line, VHDL code is generated by default.

```
makehdl('subsystst/top','HDLControlFiles',{'blackbox_ctrl.m'})
### Applying User Configuration File: blackbox_ctrl.m

### Begin Vhdl Code Generation
### Working on subsystst/top/gencode as hdlsrc/gencode.vhd
### Working on subsystst/top as hdlsrc/top.vhd
### HDL Code Generation Complete.
```

In the `makehdl` progress messages, observe that the `gencode` subsystem generates a separate code file (`gencode.vhd`) for its VHDL entity definition. The Interface subsystem does not generate such a file. The interface code for this subsystem is in `top.vhd`, generated from `subsystst/top`. The following code listing shows the component definition and instantiation generated for the Interface subsystem.

```
COMPONENT Interface
    PORT( In1 : IN    std_logic_vector(7 DOWNT0 0); -- ufix8
          In2 : IN    std_logic_vector(15 DOWNT0 0); -- ufix16
          In3 : IN    std_logic_vector(31 DOWNT0 0); -- ufix32
```

```
        Out1 : OUT  std_logic_vector(31 DOWNT0 0) -- ufix32
    );
END COMPONENT;
...
u_Interface : Interface
    PORT MAP
        (In1 => gencode_out1, -- ufix8
         In2 => gencode_out2, -- ufix16
         In3 => gencode_out3, -- ufix32
         Out1 => Interface_out1 -- ufix32
        );
    ce_out <= enb;
```

The black box interface generated for subsystems is similar to the interface generated for Model blocks, but without generation of clock signals. (See also “Generating Interfaces for Referenced Models” on page 8-6.)

## Generating Interfaces for Referenced Models

The Simulink model referencing feature allows you to include models in other models as blocks. Included models are referenced through Model blocks (see “Referencing a Model” in the Simulink documentation for detailed information).

For Model blocks, Simulink HDL Coder generates a VHDL component or a Verilog module instantiation. However, `makehdl` does not attempt to generate HDL code for the models referenced from Model blocks. You must generate HDL code for each referenced model individually. To generate code for a referenced model:

- 1 Select the referencing Model block.
- 2 Double-click the Model block to open the referenced model.
- 3 Invoke the `checkhdl` and `makehdl` functions to check and generate code from that model.

---

**Note** The `checkhdl` function does not check port data types within the referenced model.

---

The Model block is useful for multiply-instantiated blocks, or for blocks for which you already have hand-written HDL code. The generated HDL will contain all the code that is required to interface to the referenced HDL code. Code is generated with the following assumptions:

- Every HDL entity or module requires clock, clock enable, and reset ports. Therefore, these ports are defined for each generated entity or module.
- Use of Simulink data types is assumed. For VHDL code, port data types are assumed to be `STD_LOGIC` or `STD_LOGIC_VECTOR`.



## Code Generation for HDL Cosimulation Blocks

Simulink HDL Coder supports HDL code generation for the HDL Cosimulation blocks provided by the following MathWorks products:

- [Link for ModelSim](#) (this product requires the Mentor Graphics ModelSim SE/PE HDL simulator).
- [Link for Cadence Incisive](#) (this product requires the Cadence Incisive HDL simulator)

Each of the HDL Cosimulation blocks cosimulates a hardware component by applying input signals to, and reading output signals from, an HDL model that executes under an HDL simulator. For detailed information on the HDL Cosimulation blocks, see the [Link for ModelSim](#) and [Link for Cadence Incisive](#) documentation.

You can use an HDL Cosimulation block with Simulink HDL Coder to generate an interface to your hand-written or legacy HDL code. When an HDL Cosimulation block is included in a model, Simulink HDL Coder generates a VHDL or Verilog interface, depending on the selected target language.

When the target language is VHDL, the generated interface includes

- An entity definition. The entity defines ports (input, output, and clock) corresponding in name and data type to the ports configured on the HDL Cosimulation block. Clock enable and reset ports are also declared.
- An RTL architecture including a component declaration, a component configuration declaring signals corresponding to signals connected to the HDL Cosimulation ports, and a component instantiation.
- Port assignment statements as required by the model.

When the target language is Verilog, the generated interface includes

- A module defining ports (input, output, and clock) corresponding in name and data type to the ports configured on the HDL Cosimulation block. The module also defines clock enable and reset ports, and wire declarations corresponding to signals connected to the HDL Cosimulation ports.
- A module instance.

- Port assignment statements as required by the model.

The requirements for using the HDL Cosimulation block for code generation are the same as those for cosimulation. If you want to check these conditions before initiating code generation, select **Update Diagram** from the Simulink **Edit** menu.

## Generating an Interface for the Dual Port RAM Block

### In this section...

“Dual Port RAM Block Ports and Parameters” on page 8-9

“Code Generation with the Dual Port RAM Block” on page 8-11

The Dual Port RAM block lets you:

- Simulate the behavior of a dual-port RAM with registered outputs in your Simulink model.
- Generate an interface to the inputs and outputs of the RAM in HDL code.
- Generate an RTL RAM that can be inferred as a RAM by synthesis tools, for most FPGAs.

The Dual Port RAM block is in the `hdl demolib` library. To open the library, type the following command at the MATLAB prompt:

```
hdl demolib
```

Then, drag the Dual Port RAM block from the `hdl demolib` to your model, and set the block parameters and connect signals following the guidelines in “Dual Port RAM Block Ports and Parameters” on page 8-9.

### Dual Port RAM Block Ports and Parameters

The following figure shows the Dual Port RAM block.

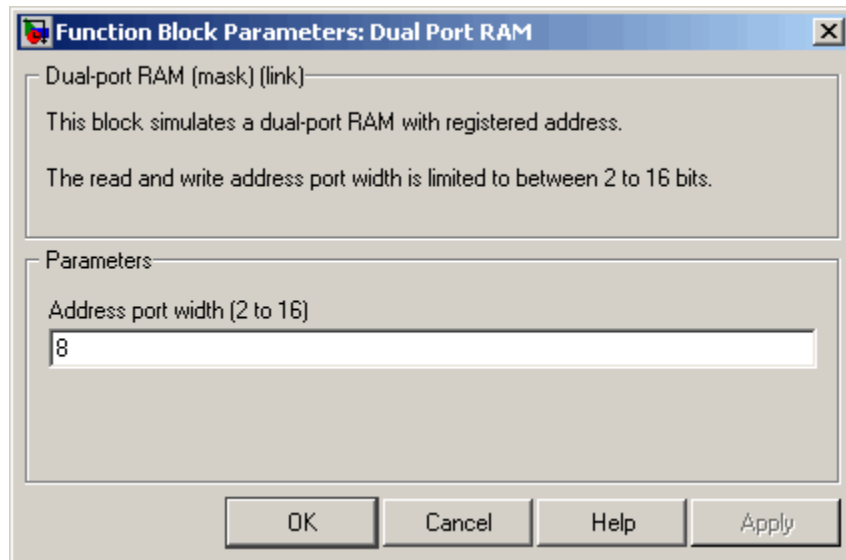


The block has the following input and output ports:

- `wr_din` : Data input. Only scalar signals can be connected to this port. The data type of the input signal must be fixed point or integer, and can be of any desired width. The port inherits the width and data type of its input signal.
- `wr_addr` , `rd_addr`: Write and read address ports, respectively. These ports are registered internally to the block.

To set the width of the address ports, enter the desired width value into the **Address port width** field of the block GUI, as shown in the following figure. The default width is 8 bits, and the maximum width is 16 bits.

The data type of signals connected to these ports must be unsigned integer (`uintN`) or unsigned fixed point (`ufixN`) with a fraction length of 0.



- `wr_en`: Write enable. This port must be connected to a Boolean signal.
- `wr_dout`, `rd_dout`: Output ports with read data for addresses `wr_addr` and `rd_addr`, respectively.

## Code Generation with the Dual Port RAM Block

When generating code for a Dual Port RAM block, note the following special considerations:

- Code generated for the Dual Port RAM block is generated to a separate file in the target directory. The naming convention for this file is *blockname.ext*, where *blockname* is derived from the name assigned to the Dual Port RAM block, and *ext* is the target language file-name extension.
- The Dual Port RAM block is implemented as a subsystem, primarily for use in simulation. When HDL code is generated for the block, a top-level interface (entity and RTL architecture) is generated; code is not generated for the underlying blocks. The generated interface is similar to the subsystem interface described in “Generating a Black Box Interface for a Subsystem” on page 8-3.

The generated interface also includes the code that implements the registered address ports (*wr\_addr*, *rd\_addr*). Because these ports are registered, data reads out from the output ports with a latency of 1 clock cycle.

- Most synthesis tools infer a RAM from the generated HDL code. However, for smaller RAM sizes, a synthesis tool may select a non-RAM alternative. Take care to verify that your synthesis tool produces the expected result when synthesizing code generated for the Dual Port RAM block.

### RAM-Based FIR Filter demo

The RAM-Based FIR Filter demo (`hdlcoderfirram.mdl`) provides an example of VHDL code generation for a Dual Port RAM block. Run this demo to acquaint yourself with the generated code.

The HDL device under test (DUT) in the model is the `FIR_RAM` subsystem. The `FIR_RAM` subsystem contains a Dual Port RAM block. The entity and architecture definitions generated for this block are written to `Dual_Port_RAM.vhd`.

The code generated for the top-level DUT, `FIR_RAM.vhd`, contains the component instantiation for the Dual Port RAM block.

## Customizing the Generated Interface

Interface generation parameters let you customize port names and other attributes of interfaces generated for the following block types:

- simulink/Ports & Subsystems/Model
- built-in/Subsystem
- lfilinklib/HDL Cosimulation
- modelsimlib/HDL Cosimulation

The following table summarizes the names, value settings, and purpose of the interface generation parameters. All parameters have string data type.

Parameter Name	Values	Description
AddClockEnablePort	'on'   'off' Default: 'on'	If 'on', add a clock enable input port to the interface generated for the block. The name of the port is specified by ClockEnableInputPort.
AddClockPort	'on'   'off' Default: 'on'	If 'on', add a clock input port to the interface generated for the block. The name of the port is specified by ClockInputPort.
AddResetPort	'on'   'off' Default: 'on'	If 'on', add a reset input port to the interface generated for the block. The name of the port is specified by ResetInputPort.
ClockEnableInputPort	Default: 'clk_enable'	Specifies HDL name for block's clock enable input port.
ClockInputPort	Default: 'clk'	Specifies HDL name for block's clock input signal.

<b>Parameter Name</b>	<b>Values</b>	<b>Description</b>
EntityName	Default: Entity name is derived from the Simulink block name, modified if necessary to generate a legal VHDL entity name.	Specifies VHDL entity or Verilog module name generated for the block.
InlineConfigurations (VHDL only)	'on'   'off' Default: If this parameter is unspecified, defaults to the value of the global InlineConfigurations property.	If 'off', suppress generation of a configurations for the block, and require a user-supplied external configuration.
ResetInputPort	Default: 'reset'	Specifies HDL name for block's reset input.
VHDLArchitectureName (VHDL only)	Default: 'RTL'	Specifies RTL architecture name generated for the block. The architecture name is generated only if InlineConfigurations = 'on'.

## Pass-Through and No-Op Implementations

Simulink HDL Coder provides special-purpose implementations that let you use a block as a wire, or simply omit a block entirely, in the generated HDL code. These implementations are summarized in the following table.

Implementation	Description
<code>hdldefaults.PassThroughHDL Emission</code>	Provides a pass-through implementation in which the block's inputs are passed directly to its outputs. (In effect, the block becomes a wire in the HDL code.)
<code>hdldefaults.NoHDL Emission</code>	Completely removes the block from the generated code. Lets you use the block in simulation but treat it as a no-op in the HDL code. You can also use this implementation as an alternative implementation for subsystems.

Simulink HDL Coder uses these implementations for many built-in blocks (such as Scopes and Assertions) that are significant in simulation but would be meaningless in HDL code.



## Limitation on Generated Verilog Interfaces

This section describes a limitation in the current release that applies to generation of Verilog interfaces for the following blocks:

- [Link for ModelSim HDL Cosimulation block](#)
- [Link for Cadence Incisive HDL Cosimulation block](#)
- Model block
- Subsystem black box implementation  
(hdldefaults.SubsystemBlackBoxHDLInstantiation)

When the target language is Verilog, only scalar ports are supported for code generation for these block types. Use of ports that are Simulink vectors on these blocks will be reported as errors on the compatibility checker (checkhdl) report, and will raise a code generator (makehdl) run-time error.



# Stateflow HDL Code Generation Support

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Overview of Stateflow HDL Code Generation (p. 9-2)

A Quick Guide to Requirements for Stateflow HDL Code Generation (p. 9-4)

Mapping Stateflow Chart Semantics to HDL (p. 9-8)

Using Mealy and Moore Machine Types in HDL Code Generation (p. 9-15)

Structuring a Model for HDL Code Generation (p. 9-24)

Design Patterns Using Advanced Stateflow Features (p. 9-30)

Introduction and pointers to demos and other information

Requirements for Stateflow charts used in HDL code generation; restrictions and limitations

How Stateflow semantics are represented in generated HDL code; rationale for restrictions on Stateflow charts that target HDL code generation

Considerations for generating HDL code from Mealy and Moore state machines

Interfacing a Stateflow chart with Simulink for HDL Code Generation

Design patterns that take advantage of advanced Stateflow features for efficient HDL code generation

## Overview of Stateflow HDL Code Generation

In this section...
“Overview” on page 9-2
“Demos and Related Documentation” on page 9-2

### Overview

Stateflow is a powerful graphical design and development tool for solving complex control and supervisory logic problems. Stateflow provides concise descriptions of complex system behavior using hierarchical finite state machine (FSM) theory, flow diagram notation, and state-transition diagrams.

You use a Stateflow chart to model a finite state machine or a complex control algorithm intended for realization as an ASIC or FPGA. When the model meets design requirements, you use Simulink HDL Coder to generate HDL code that implements the design embodied in the model. Simulink HDL Coder generates HDL code (VHDL or Verilog) from Stateflow charts. You can simulate and synthesize generated HDL code using industry standard tools, and then map your system designs into FPGAs and ASICs.

In general, generation of VHDL or Verilog code from a model containing a Stateflow chart does not differ greatly from HDL code generation from any other model. The Stateflow HDL code generator is designed to

- Support the largest possible subset of Stateflow semantics that is consistent with HDL. This broad subset lets you generate HDL code from existing models without significant remodeling effort.
- Generate bit-true, cycle-accurate HDL code that is fully compatible with Stateflow simulation semantics.

### Demos and Related Documentation

#### Demos

Simulink HDL Coder provides several demos illustrating HDL code generation from subsystems that include Stateflow charts. These demos are:

- Greatest Common Divisor
- Pipelined Configurable FIR
- 2D FDTD Behavioral Model
- CPU Behavioral Model

To open the demo models, type the following command at the MATLAB prompt:

```
demos
```

This command opens the **Help** window. In the **Demos** pane on the left, select **Simulink > Simulink HDL Coder**. Then, double-click the icon for any of the following demos, and follow the instructions in the demo window.

### **Related Documentation**

If you are familiar with Stateflow and Simulink but have not yet tried Simulink HDL Coder, see the hands-on exercises in Chapter 2, “Introduction to HDL Code Generation”.

If you are not familiar with Stateflow, see *Getting Started with Stateflow*.

For a comprehensive guide to Stateflow features, see the *Stateflow and Stateflow Coder User's Guide*.

## A Quick Guide to Requirements for Stateflow HDL Code Generation

### In this section...

“Stateflow to Simulink Interface” on page 9-4

“Data Type Usage” on page 9-4

“Chart Initialization” on page 9-5

“Registered Output” on page 9-5

“Restrictions on Imported Code” on page 9-5

“Other Restrictions” on page 9-6

This section summarizes the requirements and restrictions you should follow when configuring Stateflow charts that are intended to target HDL code generation. “Mapping Stateflow Chart Semantics to HDL” on page 9-8 provides a more detailed rationale for most of these requirements.

### Stateflow to Simulink Interface

A Stateflow chart intended for HDL code generation must be part of a Simulink subsystem. See “Structuring a Model for HDL Code Generation” on page 9-24 for an example.

### Data Type Usage

#### Supported Data Types

The current release supports a subset of MATLAB data types in Stateflow charts intended for use in HDL code generation. Supported data types are

- Signed and unsigned integer
- Double and single
- Fixed point
- Boolean

---

**Note** Multidimensional arrays of these types are supported, with the exception of data types assigned to ports. Port data types must be either scalar or vector.

---

## Chart Initialization

In Stateflow charts intended for HDL code generation, enable the chart property **Execute (enter) Chart at Initialization**. When this property is enabled, default transitions are tested and all actions reachable from the default transition taken are executed. These actions correspond to the reset process in HDL code. “Executing a Chart at Initialization” in the Stateflow documentation describes existing restrictions under this property.

The reset action must not entail the delay of combinatorial logic. Therefore, do not perform arithmetic in initialization actions.

## Registered Output

Stateflow provides the **Initialize Outputs Every Time Chart Wakes Up** chart property specifically for HDL code generation. This property lets you control whether output is persistent (stored in registers) from one sample time to the next. Such use of registers is termed *registered output*.

When the **Initialize Outputs Every Time Chart Wakes Up** option is deselected (the default), registered output is used.

When the **Initialize Outputs Every Time Chart Wakes Up** option is selected, registered output is not used. A default initial value (defined in the **Initial value** field of the **Value Attributes** pane of the Data Properties dialog box) is given to each output when the chart wakes up. This assignment guarantees that there is no reference to outputs computed in previous time steps.

## Restrictions on Imported Code

A Stateflow HDL chart must be entirely self-contained. The following restrictions apply:

- Do not call MATLAB functions other than `min` or `max`.
- Do not use MATLAB workspace data.
- Do not call C math functions
- If the **Enable C-like bit operations** property is disabled, do not use the exponentiation operator (`^`). The exponentiation operator is implemented with the C Math Library function `pow`.
- Do not include custom code. Any information entered in the Target Options dialog box is ignored.

## Other Restrictions

Simulink HDL Coder imposes a number of additional restrictions on the use of classic Stateflow features. These limitations exist because HDL does not support some features of general-purpose sequential programming languages.

- Do not define machine-parented data, machine-parented events, or local events in a Stateflow chart from which HDL code is to be generated.

Do not use the following implicit events:

- `enter`
- `exit`
- `change`

You can use the following implicit events:

- `wakeup`
- `tick`

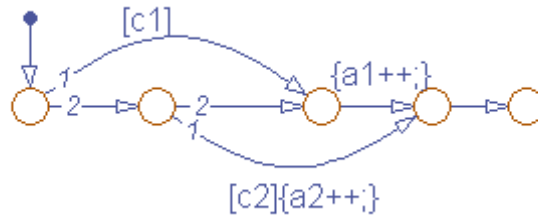
Temporal logic can be used provided the base events are limited to these types of implicit events.

- Do not use recursion through graphical functions. Simulink HDL Coder does not currently support recursion.
- Do not explicitly use loops other than `for` loops, such as in flow diagrams.

Only constant-bounded loops are supported for HDL code generation. See the Stateflow FOR Loop demo (`sf_for.mdl`) to learn how to create a `for` loop using a graphical function.



- HDL does not support a goto statement. Therefore, do not use unstructured flow diagrams, such as the flow diagram shown in the following figure.



- Do not read from output ports if outputs are not registered. (Outputs are not registered if the **Initialize Outputs Every Time Chart Wakes Up** option is selected. See also “Registered Output” on page 9-5.)
- Do not use Data Store Memory objects.
- Do not use pointer (&) or indirection (\*) operators. See the discussion of “Pointer and Address Operations” in the Stateflow documentation.
- If a Stateflow chart gets a runtime overflow error during simulation, it is possible to disable data range error checking and generate HDL code for the chart. However, in such cases Simulink HDL Coder cannot guarantee that results obtained from the generated HDL code are bit-true to results obtained from the simulation. Recommended practice is to enable overflow checking and eliminate overflow conditions from the model during simulation.

## Mapping Stateflow Chart Semantics to HDL

### In this section...

“Software Realization of Stateflow Semantics” on page 9-8

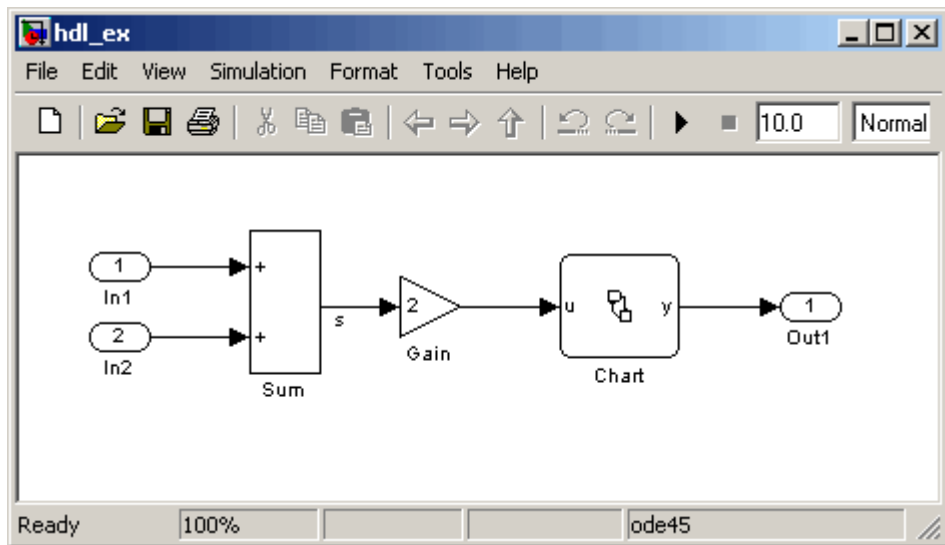
“Hardware Realization of Stateflow Semantics” on page 9-10

“Restrictions for HDL Realization” on page 9-13

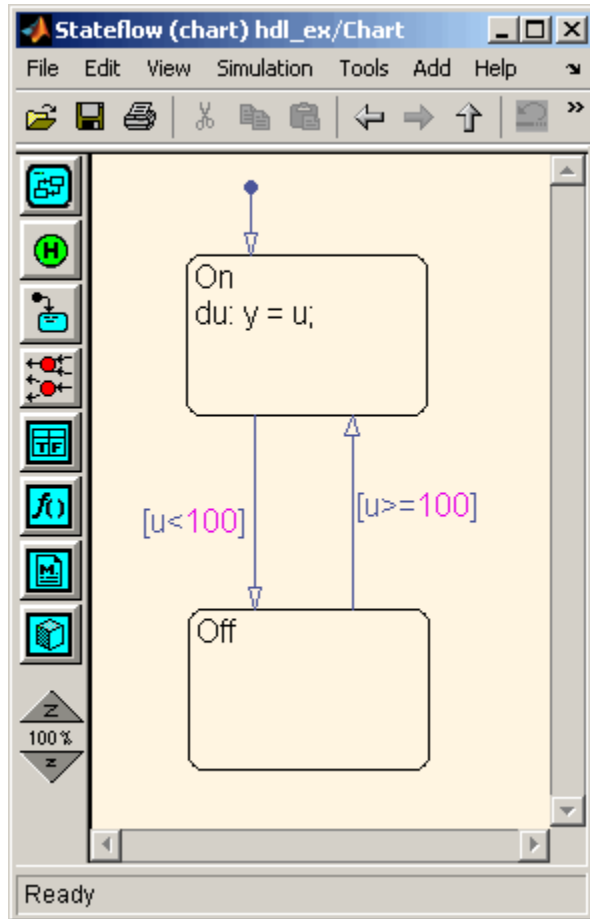
### Software Realization of Stateflow Semantics

The top-down semantics of a Stateflow chart describe how the chart executes. chart semantics describe an explicit sequential execution order for elements of the chart, such as states and transitions. These deterministic, sequential semantics map naturally to sequential programming languages, such as C. To support the rich semantics of a Stateflow chart in the Simulink environment, it is necessary to combine the state variable updates and output computation in a single function that Simulink can call.

Consider the example model shown in the following figure. The root level of the model contains three blocks (Sum, Gain and a Stateflow chart) connected in series.



The Stateflow chart from the model is shown in the following figure.



The following C code excerpt was generated by Real Time Workshop from this example model. The code illustrates how the Stateflow chart combines the output computation and state-variable update.

```

/* Output and update for atomic system: '<Root>/Chart' */
void hdl_ex_Chart(void)
{
    /* Stateflow: '<Root>/Chart' */

```

```
switch (hdl_ex_DWork.Chart.is_c1_hdl_ex) {
case hdl_ex_IN_Off:
    if (hdl_ex_B.Gain >= 100.0) {
        hdl_ex_DWork.Chart.is_c1_hdl_ex = (uint8_T)hdl_ex_IN_On;
    }

    break;

case hdl_ex_IN_On:
    if (hdl_ex_B.Gain < 100.0) {
        hdl_ex_DWork.Chart.is_c1_hdl_ex = (uint8_T)hdl_ex_IN_Off;
    } else {
        hdl_ex_B.y = hdl_ex_B.Gain;
    }

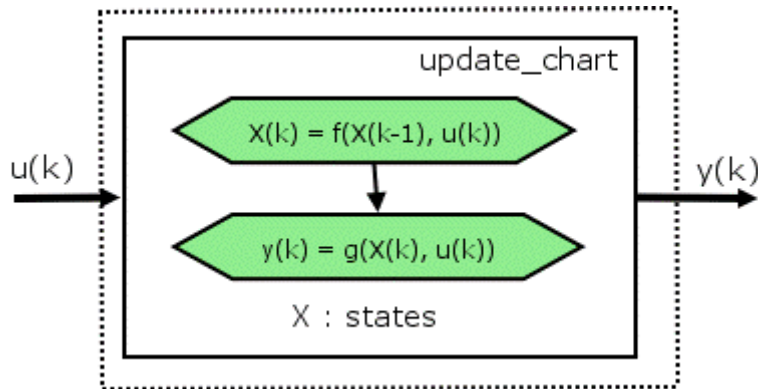
    break;

default:
    hdl_ex_DWork.Chart.is_c1_hdl_ex = (uint8_T)hdl_ex_IN_On;
    break;
}
}
```

The preceding code assigns either the state or the output, but not both. Values of output variables, as well as state, persist from one time step to another. If an output value is not assigned during a chart execution, the output simply retains its value (as defined in a previous execution).

## Hardware Realization of Stateflow Semantics

The following diagram shows a sequential implementation of Stateflow semantics for output/update computations, appropriate for targeting the C language.



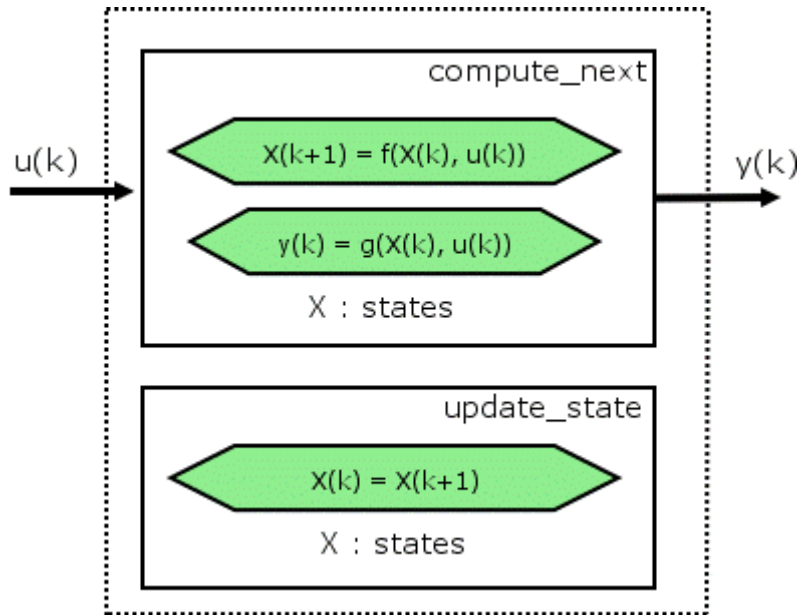
A mapping from Stateflow semantics to an HDL implementation demands a different approach. The following requirements must be met:

- **Requirement 1:** Hardware designs require separability of output and state update functions.
- **Requirement 2:** HDL is a concurrent language. To achieve the goal of bit-true simulation, execution ordering must be correct.

To meet Requirement 1, an FSM is coded in HDL as two concurrent blocks that execute under different conditions. One block evaluates the transition conditions, computes outputs and speculatively computes the next state variables. The other block updates the current state variables from the available next state and performs the actual state transitions. This second block is activated only on the trigger edge of the clock signal, or an asynchronous reset signal.

In practice, output computations usually occur more often than state updates. The presence of inputs drives the computation of outputs. State transitions occur at regular intervals (whenever the chart is activated).

The following diagram shows a concurrent implementation of Stateflow semantics for output and update computations, appropriate for targeting HDL.



The HDL code generator reuses the original single-function implementation of Stateflow semantics almost without modification. There is one important difference: instead of computing with state variables directly, all state computations are performed on local shadow variables. These variables are local to the HDL function `update_chart`. At the beginning of the `update_chart` functions, `current_state` is copied into the shadow variables. At the end of the `update_chart` function, the newly computed state is transferred to registers called collectively `next_state`. The values held in these registers are copied to `current_state` (also registered) when `update_state` is called.

By using local variables, this approach maps Stateflow sequential semantics to HDL sequential statements, avoiding the use of concurrent statements. For instance, Stateflow local variables in function scope map to VHDL variables in process scope. In VHDL, variable assignment is sequential. Therefore, statements in a Stateflow function that uses local variables can safely map to statements in a VHDL process that uses corresponding variables. The VHDL assignments execute in the same order as the assignments in the Stateflow function. The execution sequence is automatically correct.

## Restrictions for HDL Realization

Some restrictions on Stateflow usage are required to achieve a valid mapping from Stateflow to HDL code. These are summarized briefly in “A Quick Guide to Requirements for Stateflow HDL Code Generation” on page 9-4. The following sections give a more detailed rationale for most of these restrictions.

### Self-Contained Stateflow Charts

The Stateflow C target allows generated code to have some dependencies on code or data that is external to the chart. Stateflow charts intended for HDL code generation, however, must be self-contained. Observe the following rules for creating self-contained charts:

- Do not use C math functions such as `sin` and `pow`. There is no HDL counterpart to the C math library.
- Do not use calls to functions coded in M or any language other than HDL. For example, do not call M functions for a simulation target, as in the following statement:

```
ml disp( hello )
```

- Do not use custom code. Stateflow does not provide a mechanism for embedding external HDL code into Stateflow generated HDL code. Custom C code (user-written C code intended for linkage with C code generated from a Stateflow chart) is ignored during HDL code generation.

See also Chapter 8, “Interfacing Subsystems and Models to HDL Code”.

- Do not use pointer (&) or indirection (\*) operators. Pointer and indirection operators have no function in the Stateflow action language in the absence of custom code. Also, pointer and indirection operators do not map directly to synthesizable HDL.
- Do not share data (via machine-parented data or Data Store Memory blocks) between charts. Simulink HDL Coder does not map such global data to HDL, because HDL does not support global data.

### Stateflow Charts Must Not Use Features Unsupported by HDL

When creating Stateflow charts intended for HDL code generation, follow these guidelines to avoid using Stateflow language features that cannot be mapped to HDL:

- Avoid recursion. While Stateflow permits recursion (through both event processing and user-written recursive graphical functions), HDL does not allow recursion.
- Do not use Stateflow machine-parented and local events. These event types do not have equivalents in HDL. Therefore, these event types are not supported for HDL code generation.
- Avoid unstructured code. Although Stateflow allows unstructured code to be written (through transition flow diagrams and graphical functions), this usage results in goto statements and multiple function return statements. HDL does not support either goto statements or multiple function return statements.
- Select the **Execute (enter) Chart At Initialization** chart property. This option executes the update chart function immediately following chart initialization. The option is needed for HDL because outputs must be available at time 0 (hardware reset). You must select this option to ensure bit-true HDL code generation.



## Using Mealy and Moore Machine Types in HDL Code Generation

### In this section...

“Overview” on page 9-15

“Generating HDL for a Mealy Finite State Machine” on page 9-16

“Generating HDL Code for a Moore Finite State Machine” on page 9-19

### Overview

Stateflow supports modeling of three types of state machines:

- Classic (default)
- Mealy
- Moore

This section discusses issues you should consider when generating HDL code for Mealy and Moore state machines. See “Building Mealy and Moore Charts in Stateflow” in the Stateflow documentation for detailed information on Mealy and Moore state machines.

Mealy and Moore state machines differ in the following ways:

- The outputs of a Mealy state machine are a function of the current state and inputs.
- The outputs of a Moore state machine are a function of the current state only.

Moore and Mealy state charts can be functionally equivalent; an equivalent Mealy chart can derive from a Moore chart, and vice versa. A Mealy state machine has a richer description and usually requires a smaller number of states.

The principal advantages of using Mealy or Moore charts as an alternative to Classic charts are:

- Stateflow verifies the Mealy and Moore charts you create to ensure that they conform to their formal definitions and semantic rules. Stateflow reports violations at compile time (not at design time).
- Moore charts provide a more efficient implementation of Stateflow than Classic charts, for both C and HDL targets.

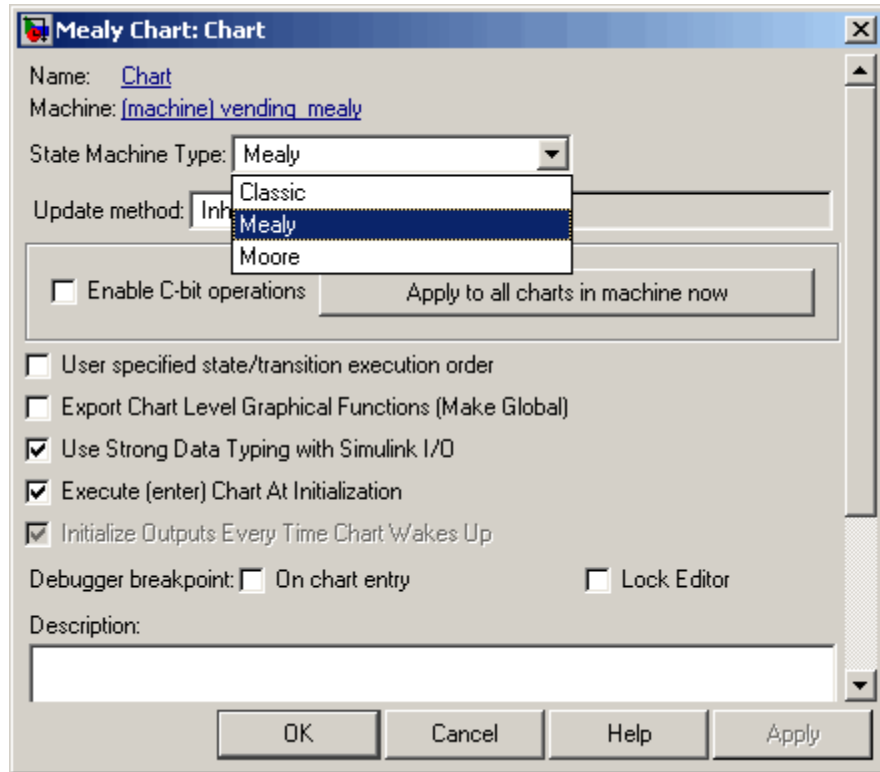
The execution of a Mealy or Moore chart at time  $t$  is the evaluation of the function represented by that chart at time  $t$ . The initialization property for output ensures that every output is defined at every time step. Specifically, the output of a Mealy or Moore chart at one time step must not depend on the output of the chart at an earlier time step.

Consider the outputs of a Stateflow chart. Stateflow permits output latching. That is, the value of an output computed at time  $t$  persists until time  $t+d$ , when it is overwritten. The output latching feature in Stateflow corresponds to registered outputs. Therefore, Mealy and Moore charts intended for HDL code generation should not use registered outputs.

### Generating HDL for a Mealy Finite State Machine

When generating HDL code for a chart that models a Mealy state machine, make sure that

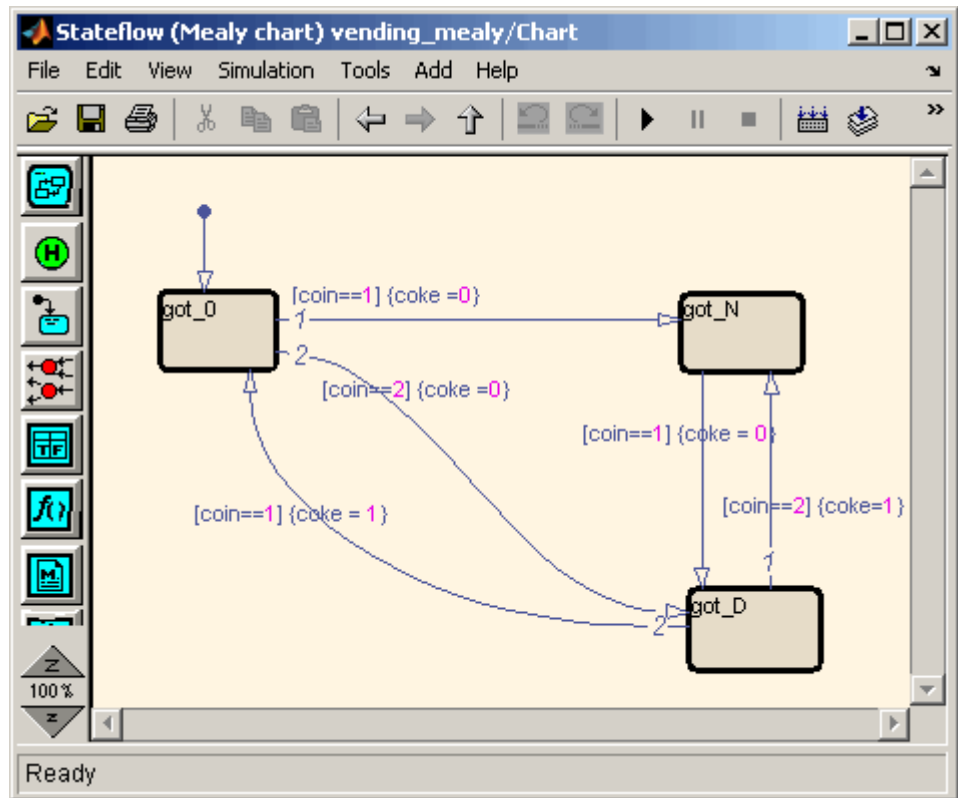
- The chart meets all general code generation requirements, as described in “A Quick Guide to Requirements for Stateflow HDL Code Generation” on page 9-4.
- The **Initialize Outputs Every Time Chart Wakes Up** option is selected. This option is selected automatically when the Mealy option is selected from the **State Machine Type** pop-up menu, as shown in the following figure.



- Actions are associated with transitions inner and outer transitions only.

Mealy actions are associated with transitions. In Mealy machines, output computation is expected to be driven by the change on inputs. In fact, the dependence of output on input is the fundamental distinguishing factor between the formal definitions of Mealy and Moore machines. The requirement that actions be given on transitions is to some degree stylistic, rather than necessary to enforce Mealy semantics. However, it is natural that output computation follows input conditions on input, because transition conditions are primarily input conditions in any machine type.

The following figure shows an example of a Stateflow chart that models a Mealy state machine.



The following code example lists the VHDL process code generated for the Mealy chart.

```

Chart : PROCESS (is_Chart, coin)
  -- local variables
  BEGIN
    is_Chart_next <= is_Chart;
    coke <= '0';

    CASE is_Chart IS
      WHEN IN_got_0 =>

        IF coin = 1.0 THEN
          coke <= '0';

```

```
        is_Chart_next <= IN_got_N;
    ELSIF coin = 2.0 THEN
        coke <= '0';
        is_Chart_next <= IN_got_D;
    END IF;

    WHEN IN_got_D =>

        IF coin = 2.0 THEN
            coke <= '1';
            is_Chart_next <= IN_got_N;
        ELSIF coin = 1.0 THEN
            coke <= '1';
            is_Chart_next <= IN_got_0;
        END IF;

    WHEN IN_got_N =>

        IF coin = 1.0 THEN
            coke <= '0';
            is_Chart_next <= IN_got_D;
        END IF;

    WHEN OTHERS =>
        is_Chart_next <= IN_got_0;
    END CASE;

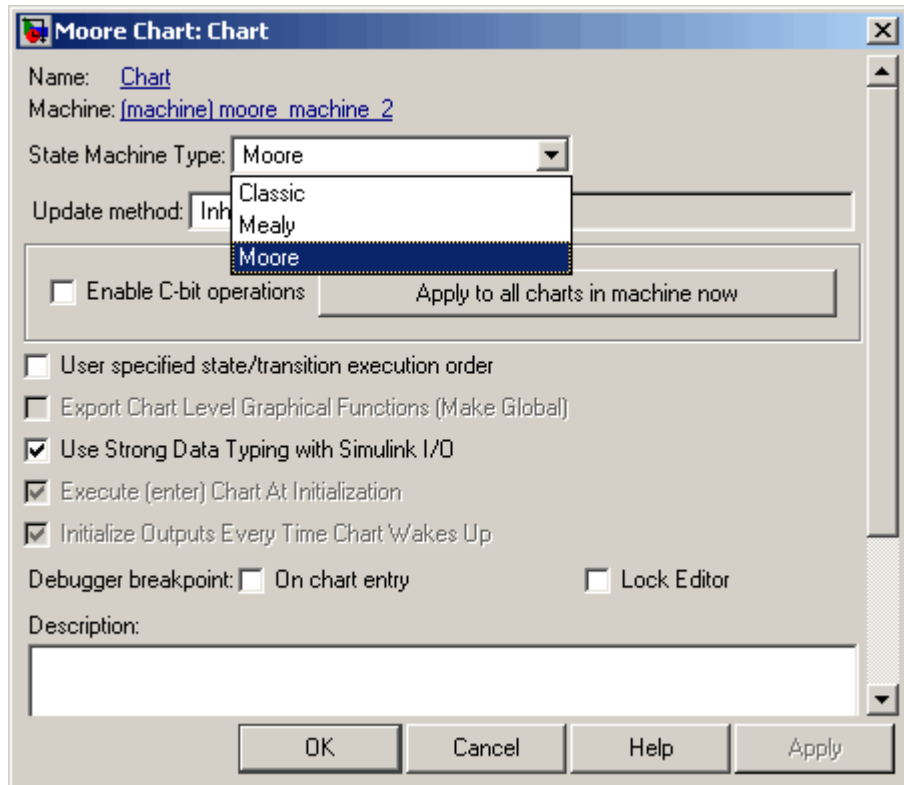
END PROCESS Chart;
```

## Generating HDL Code for a Moore Finite State Machine

When generating HDL code for a chart that models a Moore state machine, make sure that

- The chart meets all general code generation requirements, as described in “A Quick Guide to Requirements for Stateflow HDL Code Generation” on page 9-4.

- The **Initialize Outputs Every Time Chart Wakes Up** option is selected. This option is selected automatically when the Moore option is selected from the **State Machine Type** pop-up menu, as shown in the following figure.



- Actions occur in states only. These actions are unlabeled, and execute when exiting the states or remaining in the states.

Moore actions must be associated with states, because output computation must be dependent only on states, not input. Therefore, the current configuration of active states at time step  $t$  determines output. Thus, the single action in a Moore state serves as both during and exit action. If state  $S$  is active when a chart wakes up at time  $t$ , it contributes to the output whether it remains active into time  $t+1$  or not.

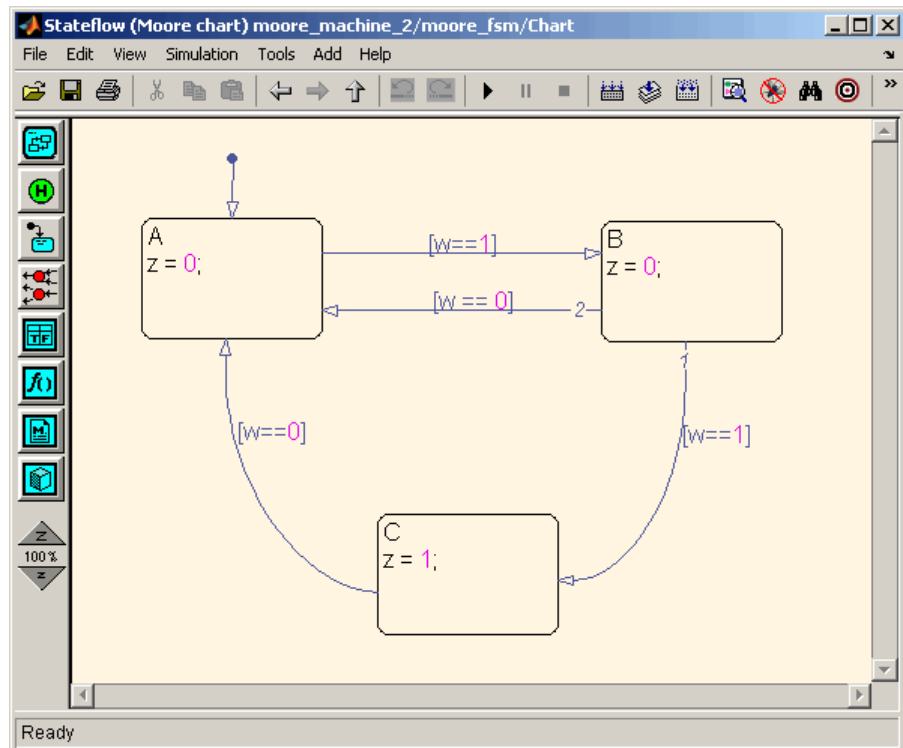
- No local data or graphical functions are used.

Function calls and local data are not allowed in a Moore chart. This ensures that output does not depend on input in ways that would be difficult for the HDL code generator to verify. These restrictions strongly encourage coding practices that separate output and input.

- No references to input occur outside of transition conditions.
- Output computation occurs only in leaf states.

This restriction guarantees that Stateflow's top-down semantics compute outputs as if actions were evaluated strictly before inner and outer flow diagrams.

The following figure shows a Stateflow chart of a Moore state machine.



The following code example illustrates generated Verilog code for the Moore chart.

```

Chart : PROCESS (is_Chart, w)
    -- local variables
    VARIABLE is_Chart_temp : T_state_type_is_Chart;
BEGIN
    is_Chart_temp := is_Chart;
    z <= '0';

    CASE is_Chart_temp IS
        WHEN IN_A =>
            z <= '0';
        WHEN IN_B =>
            z <= '0';
        WHEN IN_C =>
            z <= '1';
        WHEN OTHERS =>
            is_Chart_temp := IN_NO_ACTIVE_CHILD;
    END CASE;

    CASE is_Chart_temp IS
        WHEN IN_A =>

            IF w = '1' THEN
                is_Chart_temp := IN_B;
            END IF;

        WHEN IN_B =>

            IF w = '1' THEN
                is_Chart_temp := IN_C;
            ELSIF w = '0' THEN
                is_Chart_temp := IN_A;
            END IF;

        WHEN IN_C =>

            IF w = '0' THEN
                is_Chart_temp := IN_A;
            END IF;
    
```



```
        WHEN OTHERS =>
            is_Chart_temp := IN_A;
        END CASE;

        is_Chart_next <= is_Chart_temp;
    END PROCESS Chart;
```

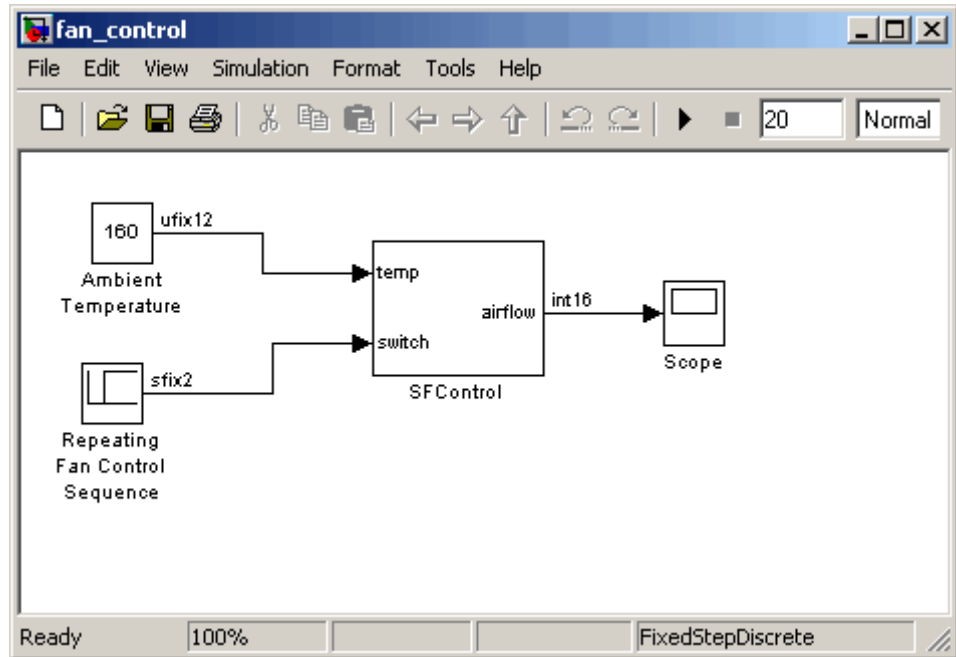
## Structuring a Model for HDL Code Generation

In general, generation of VHDL or Verilog code from a model containing a Stateflow chart does not differ greatly from HDL code generation from any other model.

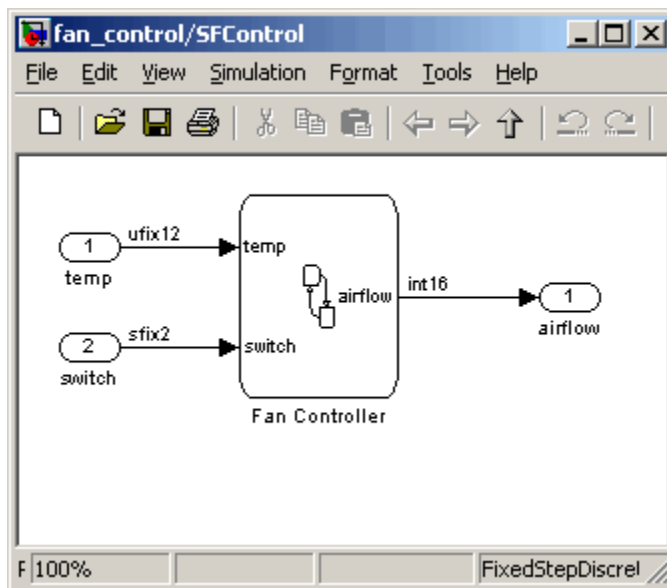
A Stateflow chart intended for HDL code generation *must* be part of a Simulink subsystem that represents the Device Under Test (DUT). The DUT corresponds to the top level VHDL entity or Verilog module for which code is generated, tested and eventually synthesized. The top level components in Simulink that drive the DUT correspond to the behavioral Simulink test bench.

You may need to restructure your models to meet this requirement. If the Stateflow chart for which you want to generate code is at the root level of your model, embed the chart in a subsystem and connect the appropriate signals to the subsystem inputs and outputs. In most cases, you can do this by simply clicking on the chart and then selecting **Edit > Create Subsystem** in the model window.

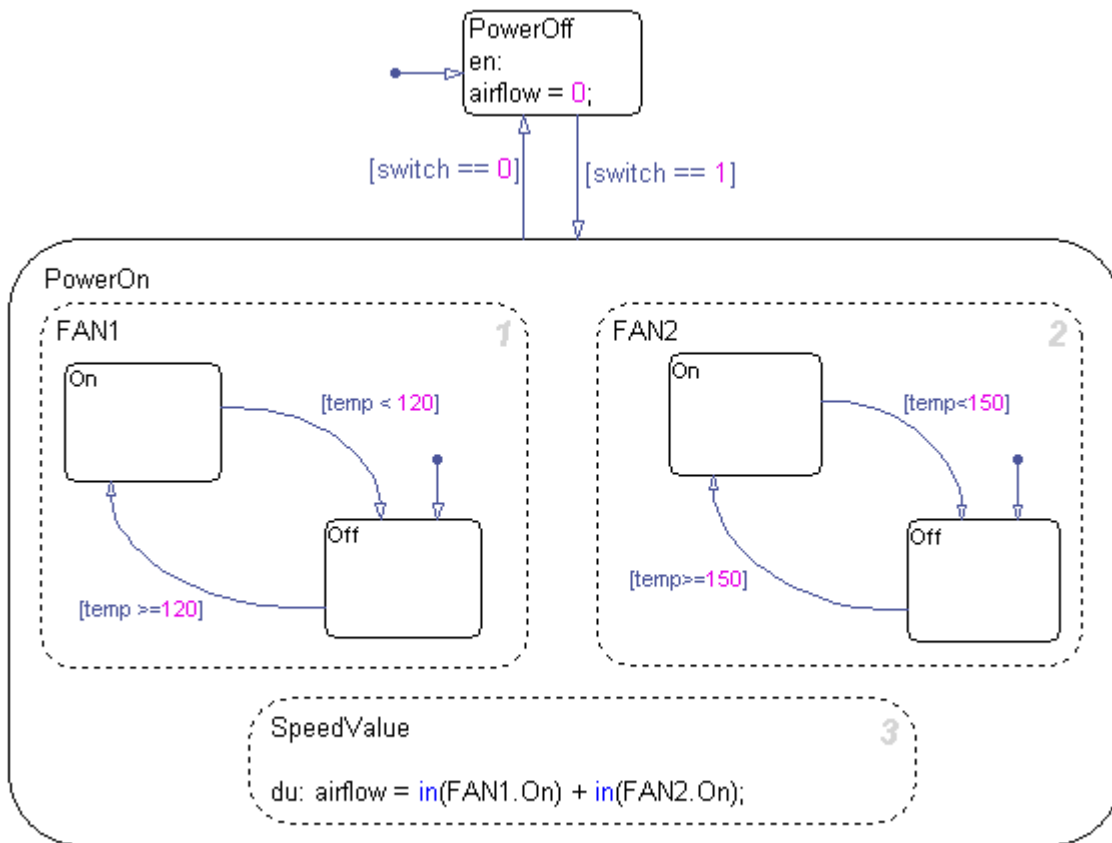
As an example of a properly structured model, consider the `fan_control` model shown in the following figure. In this model, the subsystem `SFControl` is the DUT. Two input signals drive the DUT.



The SFCControl subsystem, shown in the following figure, contains a Stateflow chart, Fan Controller. The chart that has two inputs and an output.



The Fan Controller chart, shown in the following figure, models a simple system that monitors input temperature data (temp) and turns on the two fans (FAN1 and FAN2) based on the range of the temperature. A manual override input (switch) is provided to turn the fans off forcibly. At each time step the Fan Controller outputs a value (airflow) representing the number of fans that are turned on.



The following makehdl command generates VHDL code (by default) for the subsystem containing the Stateflow chart.

```
makehdl(`fan_control/SF_Control')
```

As code generation for this subsystem proceeds, Simulink HDL Coder displays progress messages as shown in the following listing:

```
### Begin VHDL Code Generation
### Working on fan_control/SFControl as hdlsrc/SFControl.vhd
```

```
### Working on fan_control/SFControl/Fan Controller as hd1src\Fan_Controller.vhd
Stateflow parsing for model "fan_control"...Done
Stateflow code generation for model "fan_control"...Done
### HDL Code Generation Complete.
```

As the progress messages indicate, Simulink HDL Coder generates a separate code file for each level of hierarchy in the model. The following VHDL files are written to the target directory, `hd1src`:

- `Fan_Controller.vhd` contains the entity and architecture code (`Fan_Controller`) for the Stateflow chart.
- `SFControl.vhd` contains the code for the top level subsystem. This file also instantiates a `Fan_Controller` component.

Simulink HDL Coder also generates a number of other files (such as scripts for HDL simulation and synthesis tools) in the target directory. See the “HDL Code Generation Defaults” on page 14-15 for full details on generated files.

The following code excerpt shows the entity declaration generated for the `Fan_Controller` Stateflow chart in `Fan_Controller.vhd`.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;

ENTITY Fan_Controller IS
    PORT (
        clk : IN std_logic;
        clk_enable : IN std_logic;
        reset : IN std_logic;
        temp : IN std_logic_vector(11 DOWNTO 0);
        b_switch : IN std_logic_vector(1 DOWNTO 0);
        airflow : OUT std_logic_vector(15 DOWNTO 0));
END Fan_Controller;
```

This model shows the use of fixed point data types without scaling (e.g. `ufix12`, `sfix2`), as supported by Stateflow for HDL code generation. At the entity/instantiation boundary, all signals in the generated code are typed as `std_logic` or `std_logic_vector`, following general VHDL coding standard

conventions. In the architecture body, these signals are assigned to the corresponding typed signals for further manipulation and access.

## Design Patterns Using Advanced Stateflow Features

In this section...
“Temporal Logic” on page 9-30
“Graphical Function” on page 9-33
“Hierarchy and Parallelism” on page 9-35
“Stateless Charts” on page 9-39
“Truth Tables” on page 9-42

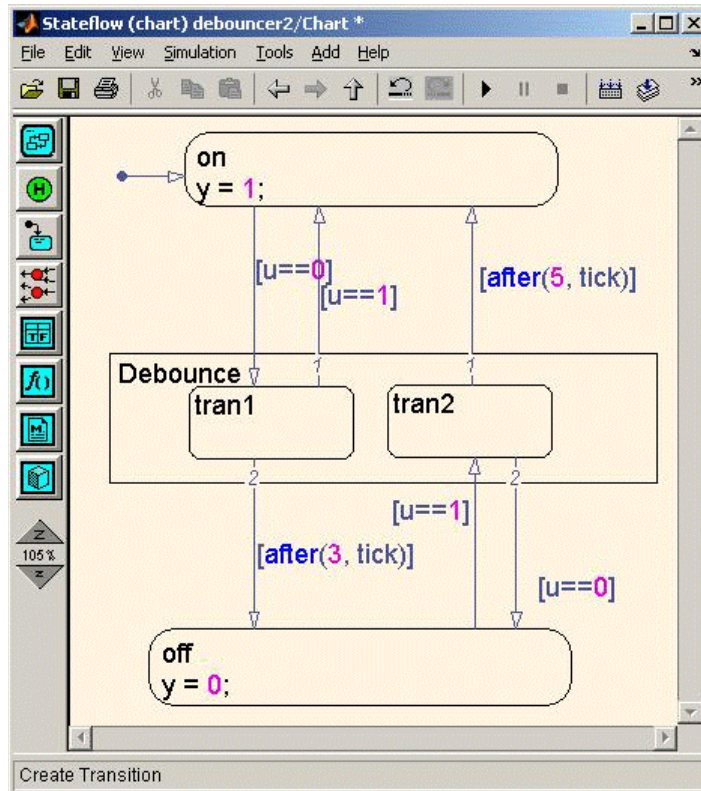
### Temporal Logic

Stateflow temporal logic operators (such as `after`, `before`, or `every`) are Boolean operators that operate on recurrence counts of Stateflow events. Temporal logic operators can appear only in conditions on transitions that from states, and in state actions. Although temporal logic does not introduce any new events into a Stateflow model, it is useful to think of the change of value of a temporal logic condition as an event. You can use temporal logic operators in many cases where a counter is required. A common use case would be to use temporal logic to implement a time-out counter.

For detailed information about Stateflow temporal logic, see “Using Temporal Logic in Actions” in the Stateflow documentation.

The chart shown in the following figure uses temporal logic in a design for a debouncer. Instead of instantaneously switching between `on` and `off` states, the chart uses two intermediate states and temporal logic to ignore transients. The transition is committed based on a time-out.





The following code excerpt shows VHDL code generated from this chart.

```

Chart : PROCESS (is_Chart, temporalCounter_i1, y_reg, u)
  -- local variables
  VARIABLE temporalCounter_i1_temp : unsigned(7 DOWNTO 0);
BEGIN
  is_Chart_next <= is_Chart;
  y_reg_next <= y_reg;
  temporalCounter_i1_temp := temporalCounter_i1;

  IF temporalCounter_i1_temp < to_unsigned(7, 8) THEN
    temporalCounter_i1_temp :=
      tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(temporalCounter_i1_temp, 9), 10)
        + tmw_to_unsigned(to_unsigned(1, 9), 10), 8);
  
```

```

END IF;

CASE is_Chart IS
  WHEN IN_tran1 =>

    IF u = '1' THEN
      is_Chart_next <= IN_on;
      y_reg_next <= '1';
    ELSIF temporalCounter_i1_temp >= to_unsigned(3, 8) THEN
      is_Chart_next <= IN_off;
      y_reg_next <= '0';
    END IF;

  WHEN IN_tran2 =>

    IF temporalCounter_i1_temp >= to_unsigned(5, 8) THEN
      is_Chart_next <= IN_on;
      y_reg_next <= '1';
    ELSIF u = '0' THEN
      is_Chart_next <= IN_off;
      y_reg_next <= '0';
    END IF;

  WHEN IN_off =>

    IF u = '1' THEN
      is_Chart_next <= IN_tran2;
      temporalCounter_i1_temp := to_unsigned(0, 8);
    END IF;

  WHEN IN_on =>

    IF u = '0' THEN
      is_Chart_next <= IN_tran1;
      temporalCounter_i1_temp := to_unsigned(0, 8);
    END IF;

  WHEN OTHERS =>
    is_Chart_next <= IN_on;

```

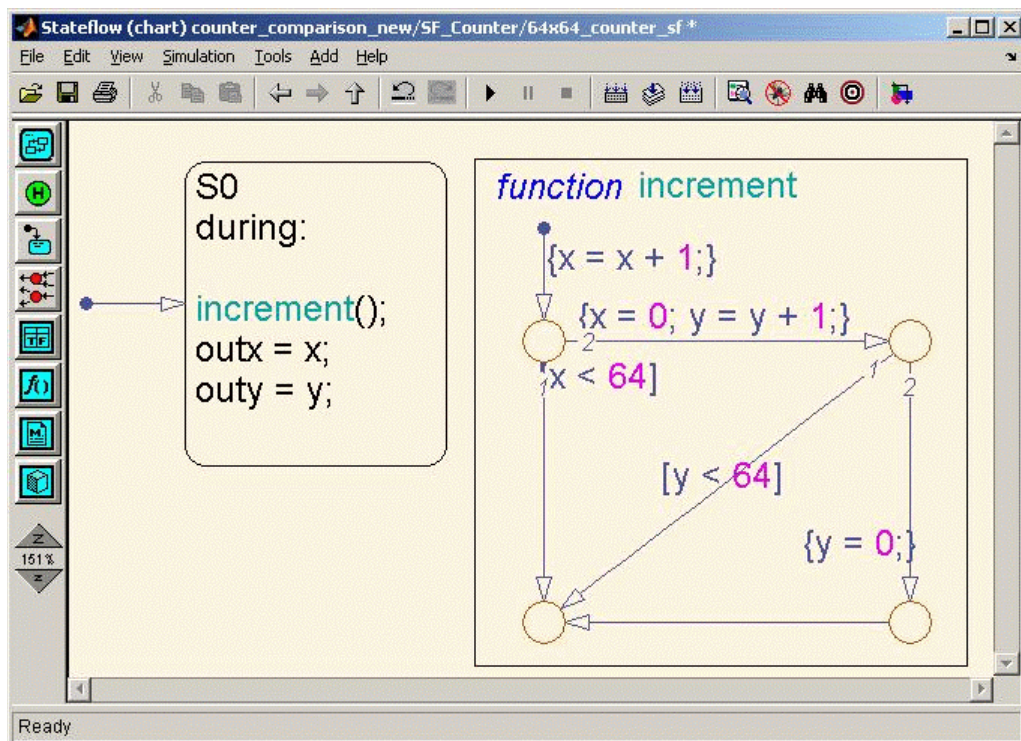
```
        y_reg_next <= '1';  
    END CASE;  
  
    temporalCounter_i1_next <= temporalCounter_i1_temp;  
END PROCESS Chart;
```

## Graphical Function

A Stateflow graphical function is a function defined graphically by a flow diagram. Graphical functions reside in a Stateflow chart along with the diagrams that invoke them. Like MATLAB and C functions, graphical functions can accept arguments and return results. Graphical functions can be invoked in transition and state actions.

The “Stateflow Notation” chapter of the Stateflow documentation includes a detailed description of graphical functions.

The following figure shows a graphical function that implements a 64-by-64 counter.



The following code excerpt shows VHDL code generated for this graphical function.

```
x64_counter_sf : PROCESS (x, y, outx_reg, outy_reg)
  -- local variables
  VARIABLE x_temp : unsigned(7 DOWNTO 0);
  VARIABLE y_temp : unsigned(7 DOWNTO 0);
BEGIN
  outx_reg_next <= outx_reg;
  outy_reg_next <= outy_reg;
  x_temp := x;
  y_temp := y;
  x_temp := tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(x_temp, 9), 10)
+ tmw_to_unsigned(to_unsigned(1, 9), 10), 8);

  IF x_temp < to_unsigned(64, 8) THEN
```

```

        NULL;
    ELSE
        x_temp := to_unsigned(0, 8);
        y_temp := tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(y_temp, 9), 10)
+ tmw_to_unsigned(to_unsigned(1, 9), 10), 8);

        IF y_temp < to_unsigned(64, 8) THEN
            NULL;
        ELSE
            y_temp := to_unsigned(0, 8);
        END IF;

    END IF;

    outx_reg_next <= x_temp;
    outy_reg_next <= y_temp;
    x_next <= x_temp;
    y_next <= y_temp;
END PROCESS x64_counter_sf;

```

## Hierarchy and Parallelism

Stateflow charts support both hierarchy (states containing other states) and parallelism (multiple states that can be active simultaneously).

Parallelism, in Stateflow, is not synonymous with concurrency. In Stateflow semantics, parallel states can be active simultaneously, but they are executed sequentially according to their execution order. (Execution order is displayed on the upper right corner of a parallel state).

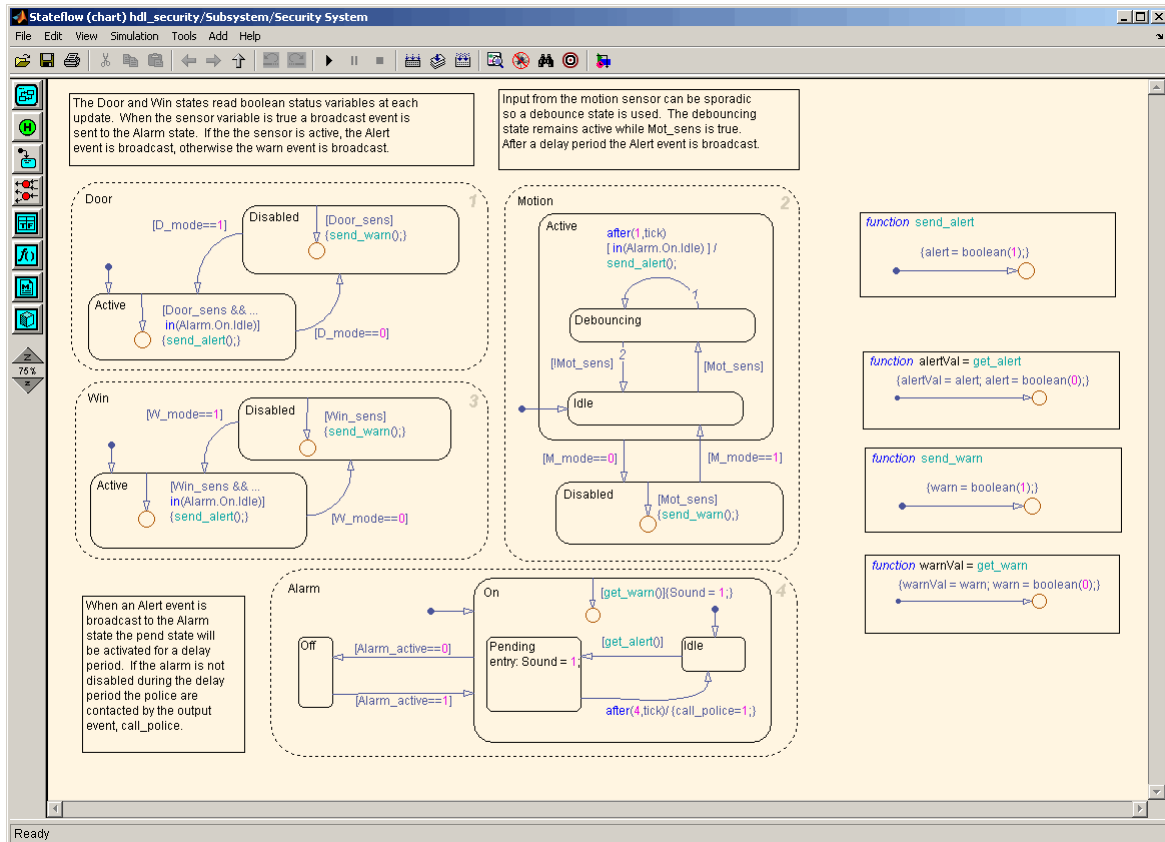
For detailed information on hierarchy and parallelism, see “Stateflow Hierarchy of Objects” and “Execution Order for Parallel States” in the Stateflow documentation.

For HDL code generation, an entire chart maps to a single output computation process. Within the output computation process:

- The execution of parallel states proceeds sequentially.
- Nested hierarchical states map to nested CASE statements in the generated HDL code.

The following figure shows a chart that models a security system. The chart contains

- Simultaneously active parallel states (in order of execution: Door, Motion, Win, Alarm).
- Hierarchy, where the parallel states contain child states. For example, the Motion state contains Active and Inactive states, and the Active state contains further nested states (Debouncing and Idle).
- Graphical functions (such as `send_alert` and `send_warn`) that set and reset flags, simulating broadcast and reception of events. These functions are used, rather than Stateflow local events, because local events are not supported for HDL code generation.



The following VHDL code excerpt was generated for the parallel Door and Motion states from this chart. The higher-level CASE statements corresponding to Door and Motion are generated sequentially to match Stateflow simulation semantics. The hierarchy of nested states maps to nested CASE statements in VHDL.

```

CASE is_Door IS
  WHEN IN_Active =>

    IF D_mode = '0' THEN
      is_Door_next <= IN_Disabled;
    ELSIF tmw_to_boolean(Door_sens AND tmw_to_stdlogic(is_On = IN_Idle)) THEN

```

```

        alert_temp := '1';
    END IF;

    WHEN IN_Disabled =>

        IF D_mode = '1' THEN
            is_Door_next <= IN_Active;
        ELSIF tmw_to_boolean(Door_sens) THEN
            warn_temp := '1';
        END IF;

    WHEN OTHERS =>
        --On the first sample call the door mode is set to active.
        is_Door_next <= IN_Active;
    END CASE;

    --This state models the modes of a motion detector sensor and implements logic
    -- to respond when that sensor is producing a signal.

    CASE is_Motion IS
        WHEN IN_Active =>

            IF M_mode = '0' THEN
                is_Active_next <= IN_NO_ACTIVE_CHILD;
                is_Motion_next <= IN_Disabled;
            ELSE

                CASE is_Active IS
                    WHEN IN_Debouncing =>

                        IF tmw_to_boolean('1'
                            AND tmw_to_stdlogic(temporalCounter_i2_temp >=
                                to_unsigned(1, 8)))
                            AND tmw_to_stdlogic(is_On = IN_Idle))
                        THEN

                            alert_temp := '1';
                            is_Active_next <= IN_Debouncing;
                            temporalCounter_i2_temp := to_unsigned(0, 8);
                        ELSIF tmw_to_boolean( NOT Mot_sens) THEN
                            is_Active_next <= b_IN_Idle;

```



```

        END IF;

    WHEN b_IN_Idle =>

        IF tmw_to_boolean(Mot_sens) THEN
            is_Active_next <= IN_Debouncing;
            temporalCounter_i2_temp := to_unsigned(0, 8);
        END IF;

    WHEN OTHERS =>
        NULL;
    END CASE;

```

## Stateless Charts

Stateflow charts consisting of pure flow diagrams (i.e., charts having no states) are useful in capturing if-then-else constructs used in procedural languages like C. The “Stateflow Notation” chapter in the Stateflow documentation discusses flow diagrams in detail.

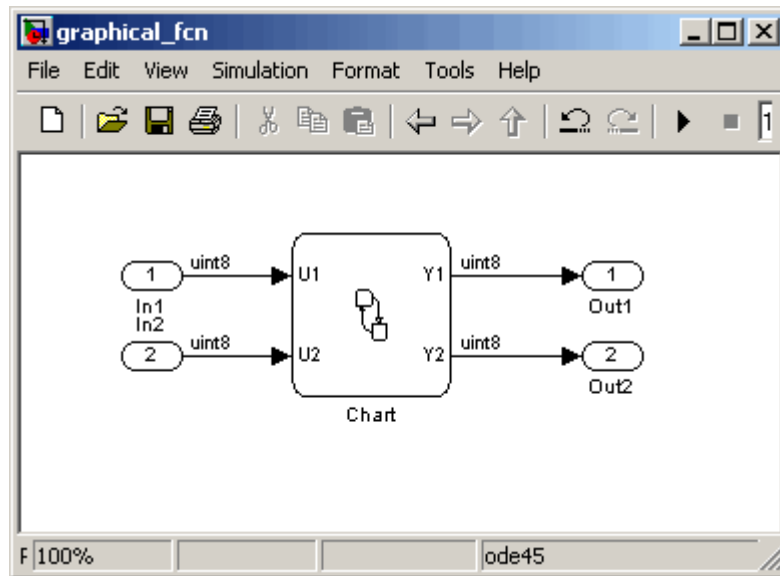
As an example, consider the following logic, expressed in C-like pseudocode.

```

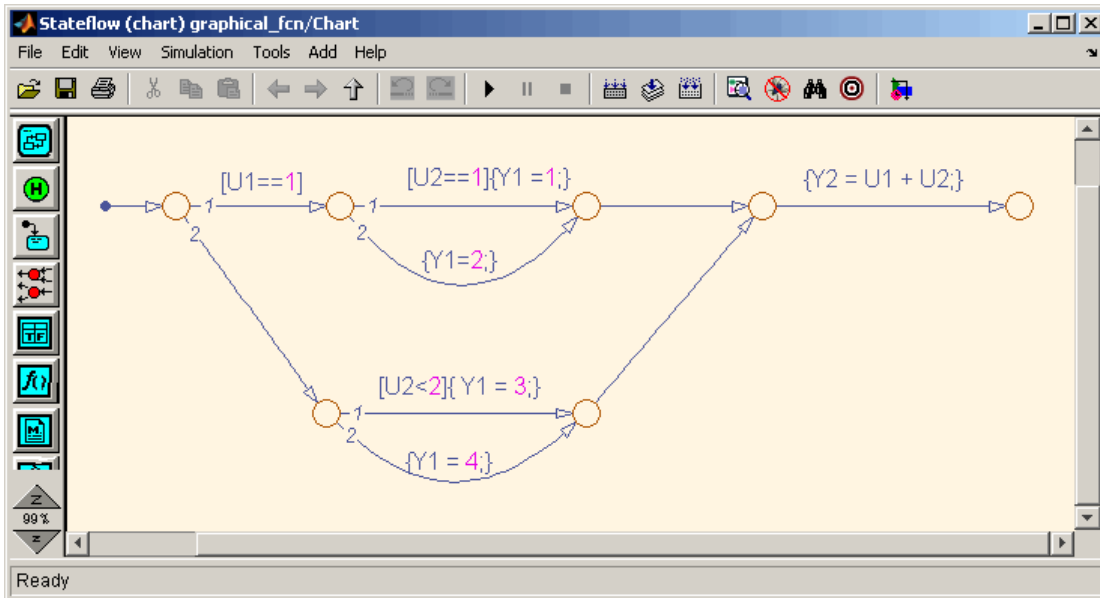
if(U1==1) {
    if(U2==1) {
        Y = 1;
    }else{
        Y = 2;
    }
}else{
    if(U2<2) {
        Y = 3;
    }else{
        Y = 4;
    }
}

```

The following figures illustrate how to model this control flow using a stateless Stateflow chart. The root model contains a subsystem and inputs and outputs to the chart.



The following figure shows the Stateflow flow diagram that implements the if-then-else logic.



The following generated VHDL code excerpt shows the nested IF-ELSE statements obtained from the flow diagram.

```

Chart : PROCESS (Y1_reg, Y2_reg, U1, U2)
  -- local variables
BEGIN
  Y1_reg_next <= Y1_reg;
  Y2_reg_next <= Y2_reg;

  IF unsigned(U1) = to_unsigned(1, 8) THEN

    IF unsigned(U2) = to_unsigned(1, 8) THEN
      Y1_reg_next <= to_unsigned(1, 8);
    ELSE
      Y1_reg_next <= to_unsigned(2, 8);
    END IF;
  END IF;

```

```
ELSIF unsigned(U2) < to_unsigned(2, 8) THEN
    Y1_reg_next <= to_unsigned(3, 8);
ELSE
    Y1_reg_next <= to_unsigned(4, 8);
END IF;

Y2_reg_next <= tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(unsigned(U1), 9),10)
+ tmw_to_unsigned(tmw_to_unsigned(unsigned(U2), 9), 10), 8);
END PROCESS Chart;
```

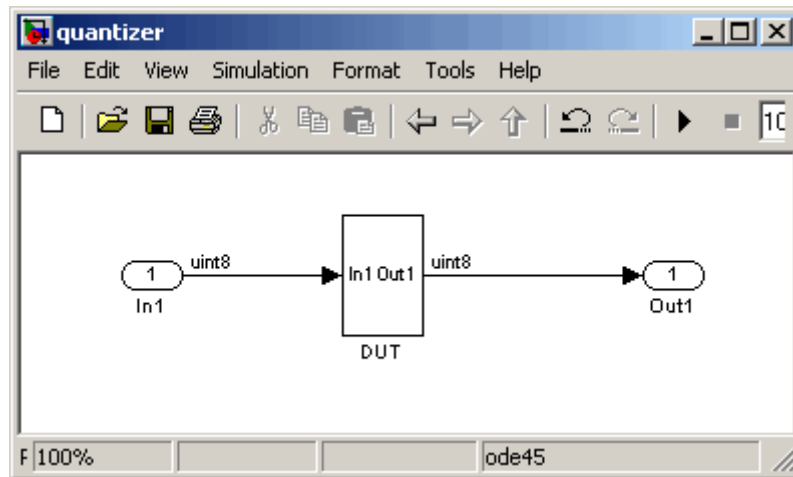
## Truth Tables

Stateflow Truth Table functions (see “Truth Table Functions” in the Stateflow documentation) are well-suited for implementing compact combinatorial logic. A typical application for Truth Tables is to implement nonlinear quantization or threshold logic. Consider the following logic:

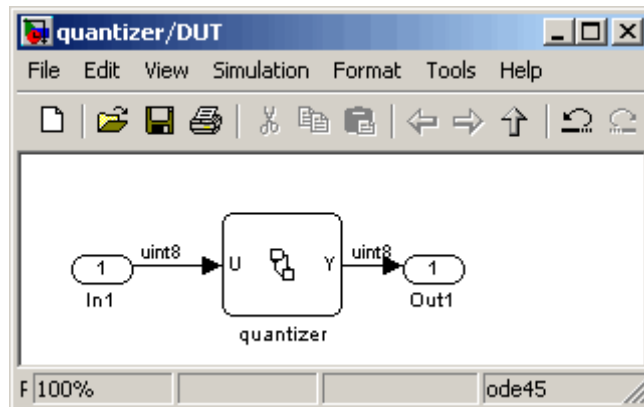
```
Y = 1 when 0 <= U <= 10
Y = 2 when 10 < U <= 17
Y = 3 when 17 < U <= 45
Y = 4 when 45 < U <= 52
Y = 5 when 52 < U
```

A stateless chart with a single call to a Truth Table function can represent this logic succinctly.

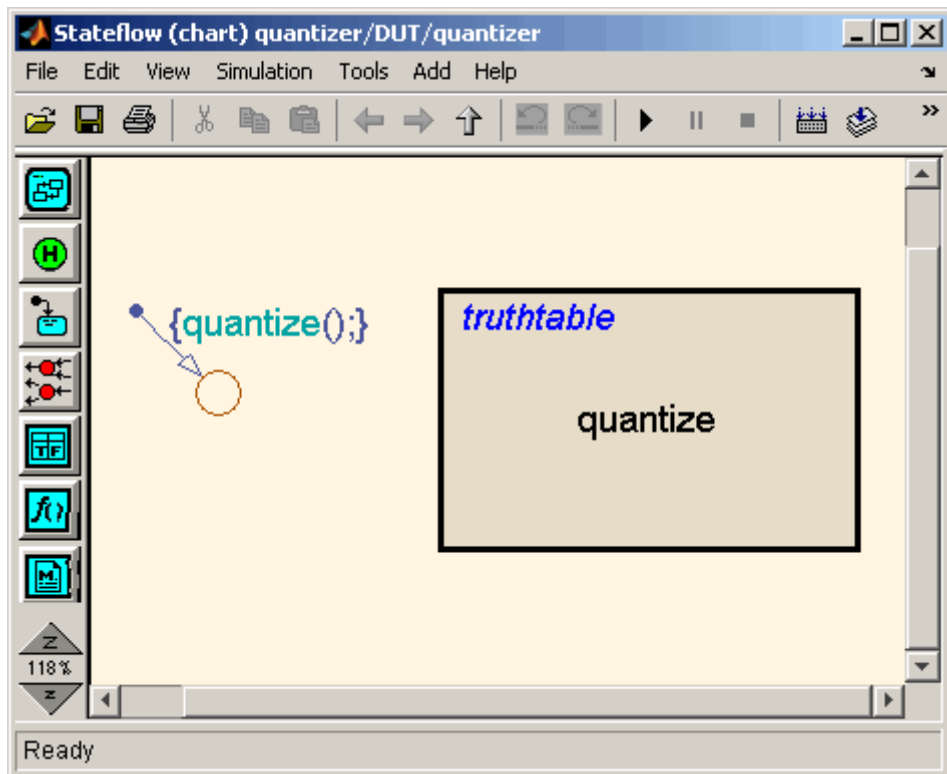
The following figure shows a model containing a subsystem, DUT.



The subsystem contains a chart, quantizer, as shown in the following figure.



The next figure shows the quantizer chart, containing the Truth Table.



The following figure shows the threshold logic, as displayed in the Truth Table Editor.

The screenshot shows the Stateflow (truth table) quantizer/DUT/quantizer.quantize Truth Table Editor. The window title is "Stateflow (truth table) quantizer/DUT/quantizer.quantize". The menu bar includes File, Edit, Settings, Add, and Help. The toolbar contains icons for Save, Print, Undo, Redo, and other editing functions.

The main area is divided into two sections: "Condition Table" and "Action Table".

**Condition Table**

	Description	Condition	D1	D2	D3	D4	D5
1		U <= 10	T	-	-	-	-
2		U <= 17	-	T	-	-	-
3		U <= 45	-	-	T	-	-
4		U <= 52	-	-	-	T	-
		Actions: Specify a row from the Action Table	1	2	3	4	5

**Action Table**

#	Description	Action
1		Y = 1
2		Y = 2
3		Y = 3
4		Y = 4
5		Y = 5

The following code excerpt shows VHDL code generated for the quantizer chart.

```
quantizer : PROCESS (Y_reg, U)
  -- local variables
  VARIABLE aVarTruthTableCondition_1 : std_logic;
  VARIABLE aVarTruthTableCondition_2 : std_logic;
  VARIABLE aVarTruthTableCondition_3 : std_logic;
  VARIABLE aVarTruthTableCondition_4 : std_logic;
BEGIN
  Y_reg_next <= Y_reg;
  -- Condition #1
  aVarTruthTableCondition_1 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(10, 8));
  -- Condition #2
  aVarTruthTableCondition_2 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(17, 8));
  -- Condition #3
  aVarTruthTableCondition_3 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(45, 8));
  -- Condition #4
  aVarTruthTableCondition_4 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(52, 8));

  IF tmw_to_boolean(aVarTruthTableCondition_1) THEN
    -- D1
    -- Action 1
    Y_reg_next <= to_unsigned(1, 8);
  ELSIF tmw_to_boolean(aVarTruthTableCondition_2) THEN
    -- D2
    -- Action 2
    Y_reg_next <= to_unsigned(2, 8);
  ELSIF tmw_to_boolean(aVarTruthTableCondition_3) THEN
    -- D3
    -- Action 3
    Y_reg_next <= to_unsigned(3, 8);
  ELSIF tmw_to_boolean(aVarTruthTableCondition_4) THEN
    -- D4
    -- Action 4
    Y_reg_next <= to_unsigned(4, 8);
  ELSE
    -- Default
    -- Action 5
    Y_reg_next <= to_unsigned(5, 8);
  END IF;
END PROCESS;
```



```
END IF;
```

```
END PROCESS quantizer;
```



# Generating HDL Code with the Embedded MATLAB Function Block

---

Introduction (p. 10-3)

Overview of the Embedded MATLAB Function block and its application in HDL code generation; pointers to related documentation and demos

Tutorial Example: Incrementer (p. 10-6)

Step-by-step tutorial shows how to incorporate an Embedded MATLAB Function block into your model for code generation

Useful Embedded MATLAB Design Patterns for HDL (p. 10-28)

Design patterns that will help you to use advanced Embedded MATLAB features

Using Fixed Point Bitwise Functions (p. 10-42)

Generating HDL code for Embedded MATLAB fixed point bitwise functions

Recommended Practices (p. 10-53)

Recommended option settings and procedures for optimal Embedded MATLAB Function block for HDL code generation

Language Support (p. 10-56)

Describes Embedded MATLAB language features supported, and restrictions that apply, when generating HDL code

Other Limitations (p. 10-66)

Describes other limitations that apply when generating HDL code with the Embedded MATLAB Function block

## Introduction

**In this section...**

“HDL Applications for the Embedded MATLAB Function Block” on page 10-3

“Related Documentation and Demos” on page 10-4

### **HDL Applications for the Embedded MATLAB Function Block**

The Embedded MATLAB Function block contains a MATLAB function in a Simulink model. The function’s inputs and outputs are represented by ports on the block, which allow you to interface your Simulink model to the function code. When you generate HDL code for an Embedded MATLAB Function block, Simulink HDL Coder generates two main HDL code files:

- A file containing entity and architecture code that implement the actual algorithm or computations generated for the Embedded MATLAB Function block.
- A file containing an entity definition and RTL architecture that provide a black box interface to the algorithmic code generated for the Embedded MATLAB Function block.

The structure of these code files is analogous to the structure of the model, in which a subsystem provides an interface between the root model and the function in the Embedded MATLAB Function block.

The Embedded MATLAB Function block supports a powerful subset of the MATLAB language that is well-suited to HDL implementation of various DSP and telecommunications algorithms, such as:

- Sequence and pattern generators
- Encoders and decoders
- Interleavers and deinterleaver
- Modulators and demodulators

- Multipath channel models; impairment models
- Timing recovery algorithms
- Viterbi algorithm; Maximum Likelihood Sequence Estimation (MLSE)
- Adaptive equalizer algorithms

## Related Documentation and Demos

The following documentation and demos provide further information on the Embedded MATLAB Function block.

### Related Documentation

For general documentation on the Embedded MATLAB Function block, see:

- “Using the Embedded MATLAB Function Block” in the Simulink documentation
- Embedded MATLAB Function block reference in the Simulink documentation

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder supports most of the fixed-point runtime library functions supported by Embedded MATLAB™. See “Working with the Fixed-Point Embedded MATLAB™ Subset” in the Fixed Point Toolbox documentation for a complete list of these functions, and general information on limitations that apply to the use of Fixed-Point Toolbox with Embedded MATLAB.

### Demos

The `hdlcoderviterbi2.mdl` demo models a Viterbi decoder, incorporating an Embedded MATLAB Function block for use in simulation and HDL code generation. To open the model, type the following command at the MATLAB command line:

```
hdlcoderviterbi2
```

The `hdlcodercpu_eml.mdl` demo models a CPU with a Harvard RISC architecture, incorporating many Embedded MATLAB Function blocks to simulate and generate code for CPU and memory elements. To open the model, type the following command at the MATLAB command line:

hdlcodercpu\_em1

## Tutorial Example: Incrementer

### In this section...

“Example Model Overview” on page 10-6

“Setting Up” on page 10-9

“Creating the Model and Configuring General Model Settings” on page 10-10

“Adding an Embedded MATLAB Function Block to the Model” on page 10-11

“Setting Optimal Fixed Point Options for the Embedded MATLAB Function Block” on page 10-12

“Programming the Embedded MATLAB Function” on page 10-14

“Constructing and Connecting the DUT\_eML\_Block Subsystem” on page 10-17

“Compiling the Model and Displaying Port Data Types” on page 10-23

“Simulating the eml\_hdl\_incrementer Model” on page 10-23

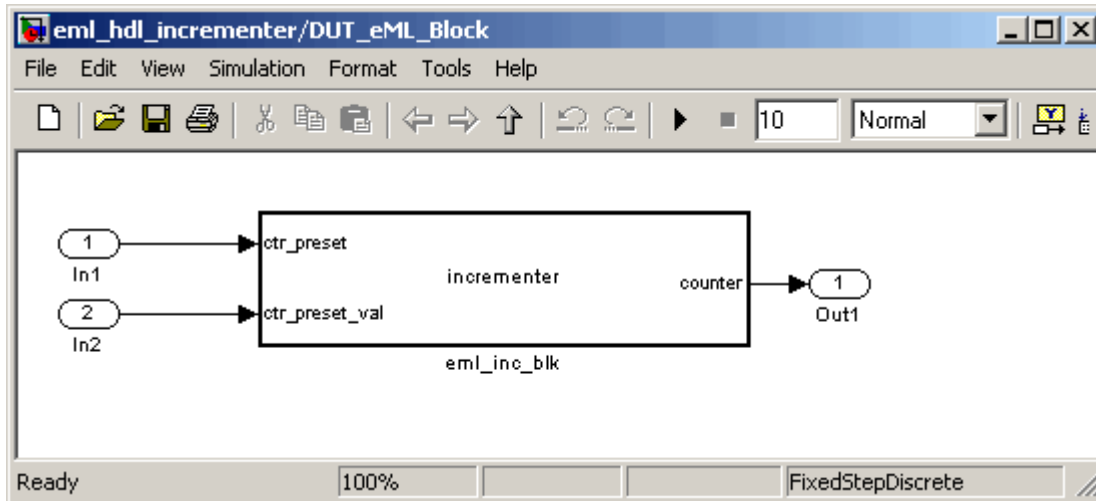
“Generating HDL Code” on page 10-24

### Example Model Overview

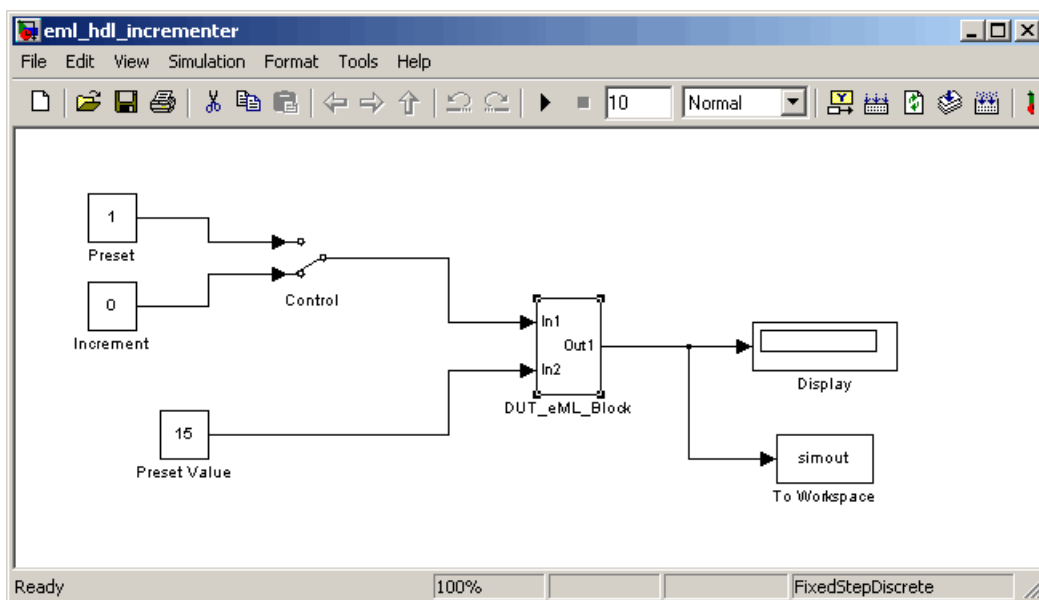
In this tutorial, you construct and configure a simple model, `eml_hdl_incrementer`, and then generate VHDL code from the model. `eml_hdl_incrementer` includes an Embedded MATLAB Function block that implements a simple fixed-point counter function, `incrementer`. The `incrementer` function is invoked once during each sample period of the model. The function maintains a persistent variable count, which is either incremented or reinitialized to a preset value (`ctr_preset_val`), depending on the value passed in to the `ctr_preset` input of the Embedded MATLAB Function block. The function returns the counter value (`counter`) at the output of the Embedded MATLAB Function block.

The Embedded MATLAB Function block is contained in a subsystem, `DUT_eML_Block`. The subsystem functions as the device under test (DUT) from which HDL code is generated. The following figure shows the subsystem.





The root-level model drives the subsystem and includes Display and To Workspace blocks for use in simulation. (The Display and To Workspace blocks do not generate any HDL code.) The following figure shows the model.



---

**Tip** If you do not want to construct the model step by step, or do not have time, the example model is available in the Simulink HDL Coder demos directory as the following file:

```
MATLABROOT\toolbox\hdlcoder\hdlcoderdemos\em1_hdl1_incrementer.mdl
```

---

## The Incrementer Function Code

The following code listing gives the complete incrementer function definition:

```
function counter = incrementer(ctr_preset, ctr_preset_val)
% The function incrementer implements a preset counter that counts
% how many times this block is called.
%
% This example function shows how to model memory with persistent variables,
% using fimath settings suitable for HDL. It also demonstrates MATLAB
% operators and other language features that Simulink HDL Coder supports
% for code generation from Embedded MATLAB Function blocks.
%
% On the first call, the result 'counter' is initialized to zero.
% The result 'counter' saturates if called more than 2^14-1 times.
% If the input ctr_preset receives a nonzero value, the counter is
% set to a preset value passed in to the ctr_preset_val input.

persistent current_count;
if isempty(current_count)
    % zero the counter on first call only
    current_count = uint32(0);
end

counter = getfi(current_count);

if ctr_preset
    % set counter to preset value if input preset signal is nonzero
    counter = ctr_preset_val;
else
```

```

    % otherwise count up
    inc = counter + getfi(1);
    counter = getfi(inc);
end

% store counter value for next iteration
current_count = uint32(counter);

function hdl_fi = getfi(val)

nt = numerictype(0,14,0);
fm = fimath('OverflowMode', 'saturate', ...
           'RoundMode', 'floor', ...
           'ProductMode', 'FullPrecision', ...
           'ProductWordLength', 32,...
           'SumMode', 'FullPrecision', ...
           'SumWordLength', 32);

hdl_fi = fi(val, nt, fm);

```

## Setting Up

Before you begin building the example model, set up a working directory and (if necessary), build an HDL supported blocks library, as described in the following sections.

### Setting Up a Directory

- 1 Start MATLAB.
- 2 Create a directory named `eml_tut`, for example:

```
mkdir D:\work\eml_tut
```

The `eml_tut` directory stores the model you create, and also contains directories and code generated by Embedded MATLAB and Simulink HDL Coder. The location of the directory does not matter, except that it should not be within the MATLAB directory tree.

- 3 Make the `eml_tut` directory your working directory, for example:

```
cd D:\work\eml_tut
```

## Creating the Model and Configuring General Model Settings

In this section, you create a model and set some parameters to values recommended for HDL code generation, using the Simulink HDL Coder M-file utility, `hdlsetup.m`. The `hdlsetup` command uses the Simulink `set_param` function to set up models for HDL code generation quickly and consistently. See “Initializing Model Parameters with `hdlsetup`” on page 2-7 for further information about `hdlsetup`.

To set the model parameters:

- 1 Create a new Simulink model.
- 2 Save the model as `eml_hdl_incrementer.mdl`.
- 3 At the MATLAB command prompt, type:

```
hdlsetup('eml_hdl_incrementer')
```

- 4 Select **Configuration Parameters** from the **Simulation** menu in the `eml_hdl_incrementer` model window.

The Configuration Parameters dialog box opens with the **Solver** options pane displayed.

- 5 Set the following **Solver** options, which are useful in simulating this model:

**Fixed step size** : 1.

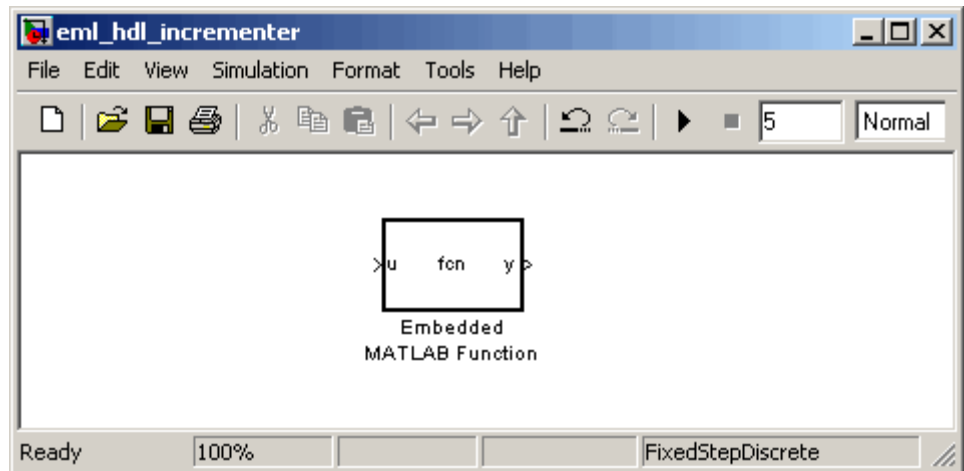
**Stop time** : 5.

- 6 Click **Apply**. Then close the Configuration Parameters dialog box.1.
- 7 Select **Save** from the Simulink **File** menu, to save the model with its new settings.

## Adding an Embedded MATLAB Function Block to the Model

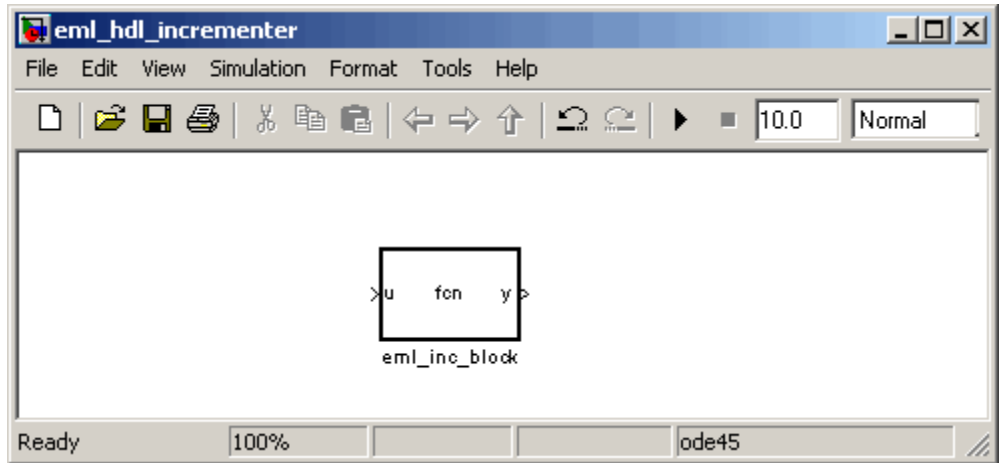
- 1 Open the Simulink Library Browser. Then, select the Simulink/User-Defined Functions sublibrary.
- 2 Select the Embedded MATLAB Function block from the library window and add it to the Simulink model.

The model should now appear as shown on the following figure:



- 3 Change the block label from Embedded MATLAB Function to eml\_inc\_block.

The model should now appear as shown on the following figure:



- 4 Save the model.
- 5 Close the hdlsupported library window.

### Setting Optimal Fixed Point Options for the Embedded MATLAB Function Block

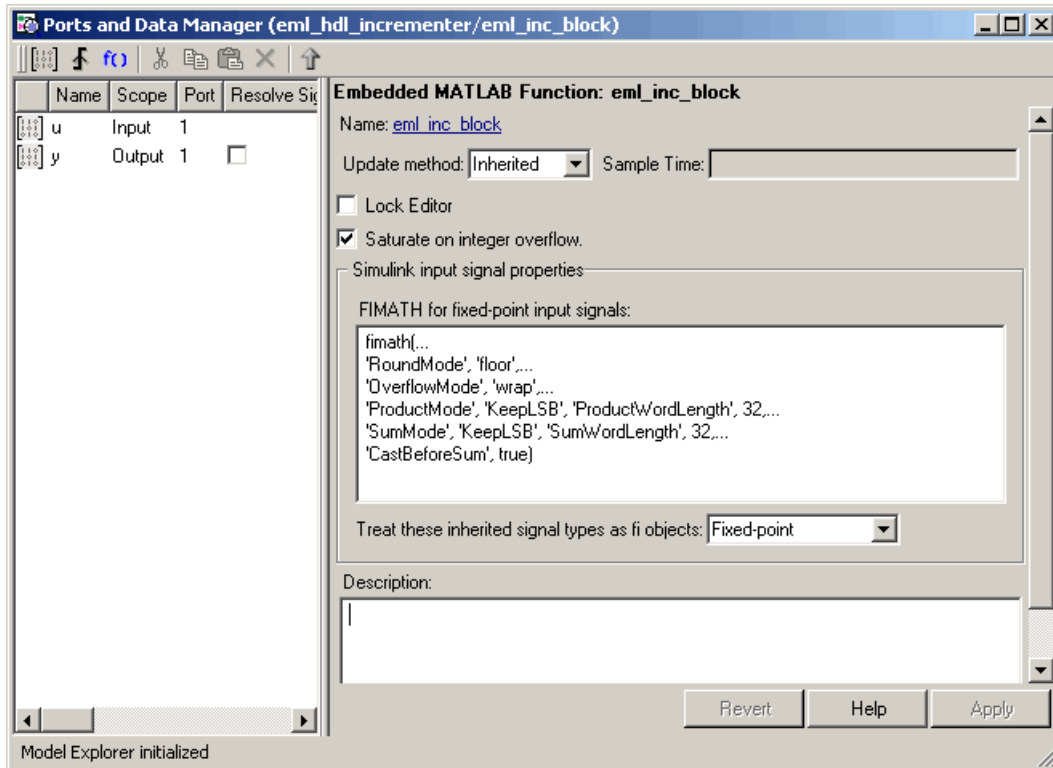
This section describes how to set up the FIMATH specification and other fixed point options that are recommended for efficient HDL code generation from the Embedded MATLAB Function block. The recommended settings are

- ProductMode property of the FIMATH specification: 'FullPrecision'
- SumMode property of the FIMATH specification: 'FullPrecision'
- **Treat these inherited signal types as fi objects** option: Fixed-point (This is the default setting.)

Configure the options as follows:

- 1 If it is not already open, open the `eml_hdl_incrementer` model that you created in “Adding an Embedded MATLAB Function Block to the Model” on page 10-11.
- 2 Double-click the Embedded MATLAB Function block to open it for editing. The Embedded MATLAB Editor appears.

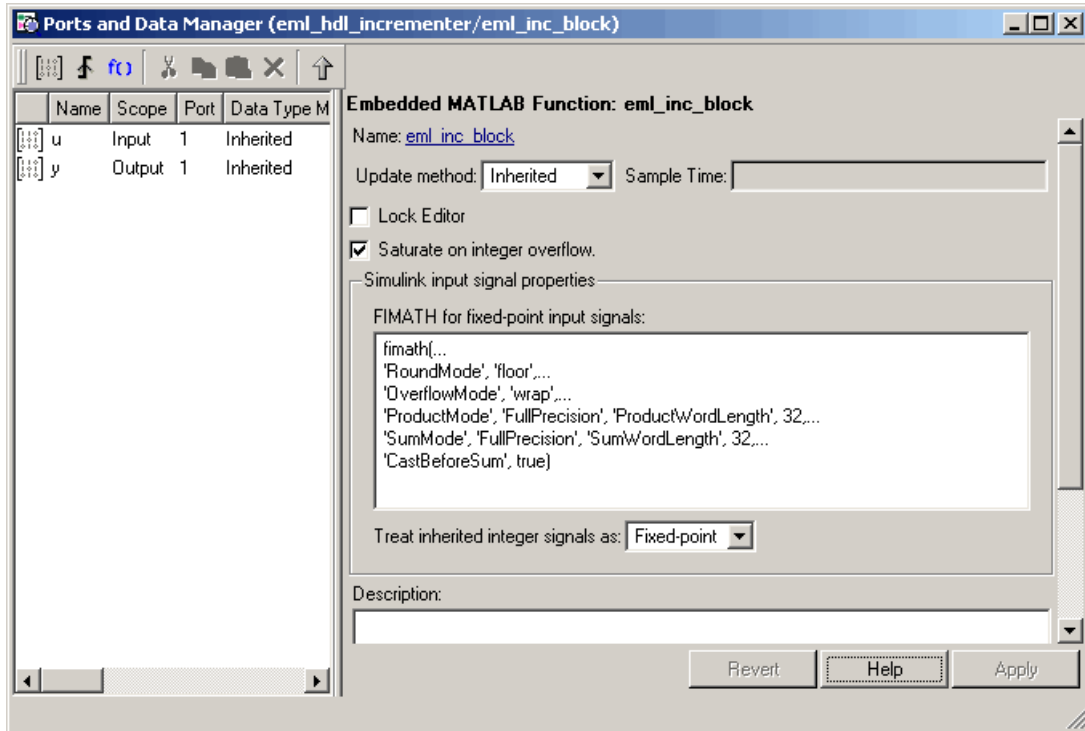
- 3** Select **Edit Data/Ports** from the Tools menu. The Ports and Data Manager dialog box opens, displaying the default FIMATH specification and other properties for the Embedded MATLAB Function block.



- 4** Replace the default **FIMATH for fixed-point signals** specification with the following:

```
fimath(...
'RoundMode', 'floor',...
'OverflowMode', 'wrap',...
'ProductMode', 'FullPrecision', 'ProductWordLength', 32,...
'SumMode', 'FullPrecision', 'SumWordLength', 32,...
'CastBeforeSum', true)
```

- 5 Click **Apply**. The Embedded MATLAB Function block properties should now appear as shown in the following figure.



- 6 Close the Ports and Data Manager dialog box.

- 7 Save the model.

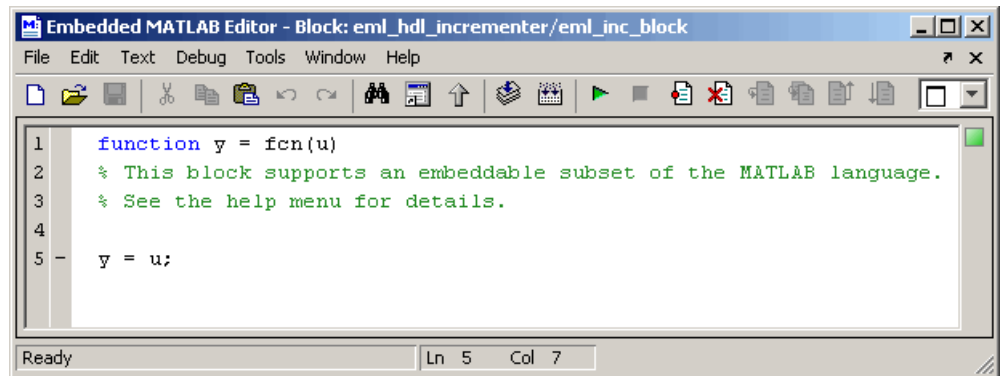
## Programming the Embedded MATLAB Function

The next step is add code to the Embedded MATLAB Function block to define the incremter function, and then use MATLAB diagnostics to check for errors.

Use the following steps to program the function:



- 1 If not already open, open the `eml_hdl_incrementer` model that you created in “Adding an Embedded MATLAB Function Block to the Model” on page 10-11.
- 2 Double-click the Embedded MATLAB Function block to open it for editing. The Embedded MATLAB Editor appears. The editor displays a default function definition, as shown in the following figure.



The screenshot shows the Embedded MATLAB Editor window titled "Embedded MATLAB Editor - Block: eml\_hdl\_incrementer/eml\_inc\_block". The window has a menu bar with "File", "Edit", "Text", "Debug", "Tools", "Window", and "Help". Below the menu bar is a toolbar with various icons for file operations, editing, and execution. The main text area contains the following code:

```
1 function y = fcn(u)
2     % This block supports an embeddable subset of the MATLAB language.
3     % See the help menu for details.
4
5 - y = u;
```

The status bar at the bottom of the window shows "Ready" and "Ln 5 Col 7".

The next step is to replace the default function with the incrementer function.

- 3 Click **Select All** in the **Edit** menu of the Embedded MATLAB Editor window. Then, delete all the default code.
- 4 Copy the complete incrementer function definition from the listing given in “The Incrementer Function Code” on page 10-8, and paste it into the Embedded MATLAB Editor.

The Embedded MATLAB Editor should appear as shown in the following figure:

```

Embedded MATLAB Editor - Block: eml_hdl_incrementer/eml_inc_block
File Edit Text Debug Tools Window Help
1 function counter = incrementer(ctr_preset, ctr_preset_val)
2 % The function incrementer implements a preset counter that counts
3 % how many times this block is called.
4 %
5 % This example function shows how to model memory with persistent variables,
6 % using fimath settings suitable for HDL. It also demonstrates MATLAB
7 % operators and other language features that Simulink HDL Coder supports
8 % for code generation from Embedded MATLAB Function blocks.
9 %
10 % On the first call, the result 'counter' is initialized to zero.
11 % The result 'counter' saturates if called more than 2^14-1 times.
12 % If the input ctr_preset receives a nonzero value, the counter is
13 % set to a preset value passed in to the ctr_preset_val input.
14
15 persistent current_count;
16 if isempty(current_count)
17     % zero the counter on first call only
18     current_count = uint32(0);
19 end
20
21 counter = getfi(current_count);
22
23 if ctr_preset
24     % set counter to preset value if input preset signal is nonzero
25     counter = ctr_preset_val;
26 else
27     % otherwise count up
28     inc = counter + getfi(1);
29     counter = getfi(inc);
30 end
31
32 % store counter value for next iteration
33 current_count = uint32(counter);
34
35 function hdl_fi = getfi(val)
36
37 nt = numerictype(0,14,0);
38 fm = fimath('OverflowMode', 'saturate', ...
39           'RoundMode', 'floor', ...
40           'ProductMode', 'FullPrecision', ...
41           'ProductWordLength', 32,...
42           'SumMode', 'FullPrecision', ...
43           'SumWordLength', 32);
44
45 hdl_fi = fi(val, nt, fm);

```

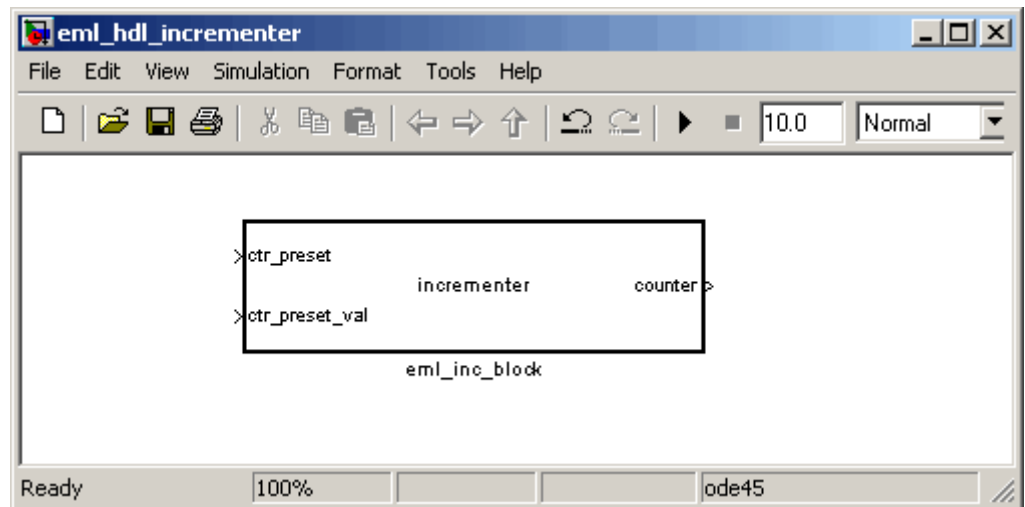
Ready Ln 13 Col 63

**5** Select **Save Model** from the **File** menu in the Embedded MATLAB Editor.

Saving the model updates the Simulink window, redrawing the Embedded MATLAB Function block.

Changing the function header of the Embedded MATLAB Function block makes the following changes to the Embedded MATLAB Function block in the Simulink model:

- The function name in the middle of the block changes to `incrementer`
  - The arguments `ctr_preset` and `ctr_preset_val` appear as input ports to the block.
  - The return value `counter` appears as an output port from the block.
- 6 Resize the block to make the port labels more legible. The model should now resemble the following figure.



- 7 Save the model again.

## Constructing and Connecting the DUT\_eML\_Block Subsystem

This section assumes that you have completed “Programming the Embedded MATLAB Function” on page 10-14 with a successful build. In this section, you construct a subsystem containing the `incrementer` function block, to be used as the device under test (DUT) from which HDL code is generated. You then set the port data types and connect the subsystem ports to the model.

### Constructing the DUT\_eML\_Block Subsystem

Construct a subsystem containing the incremter function block as follows:

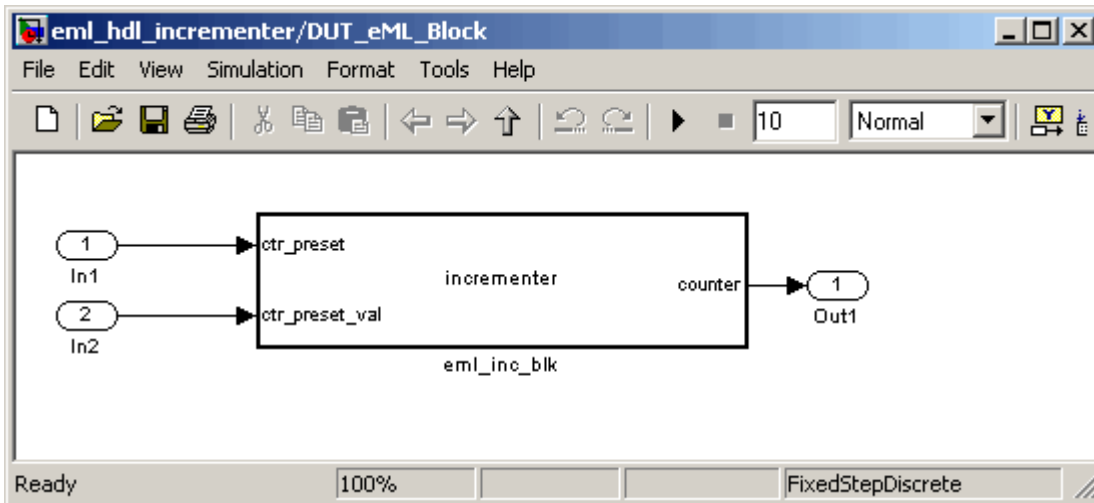
- 1 Click on the incremter function block.
- 2 From the Simulink **Edit** menu, select **Create Subsystem**.

A subsystem, labeled Subsystem, is created in the model window.

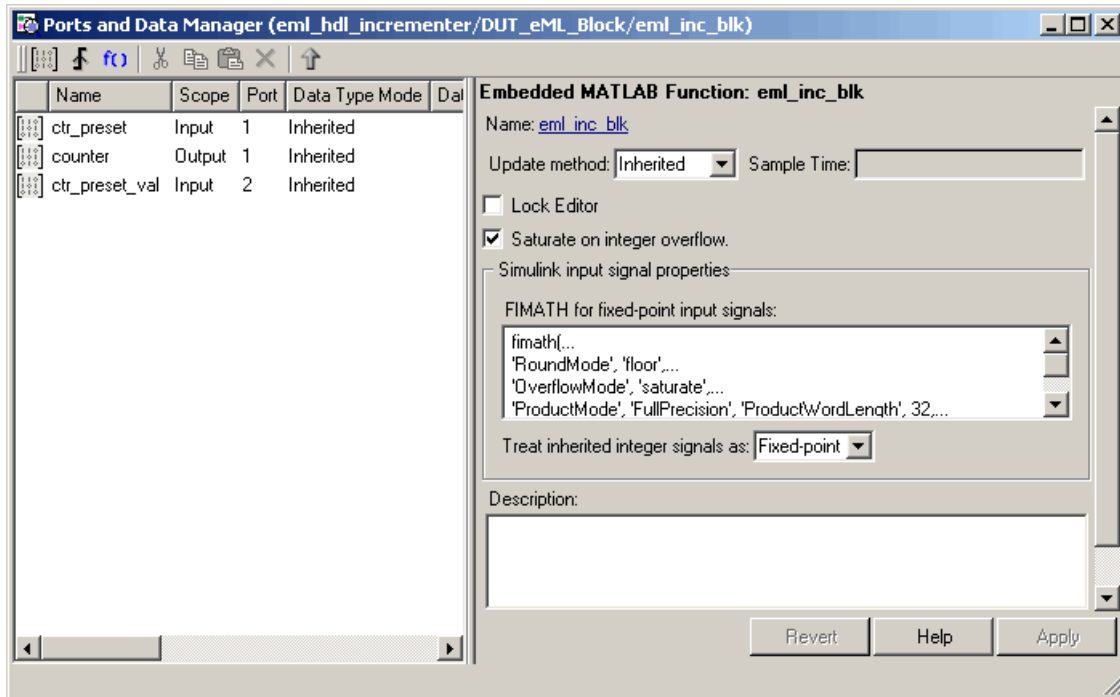
- 3 Change the Subsystem label to DUT\_eML\_Block.

### Setting Port Data Types for the Embedded MATLAB Function block

- 1 Double-click the subsystem to view its interior. As shown in the following figure, the subsystem contains the incremter function block, with input and output ports connected.

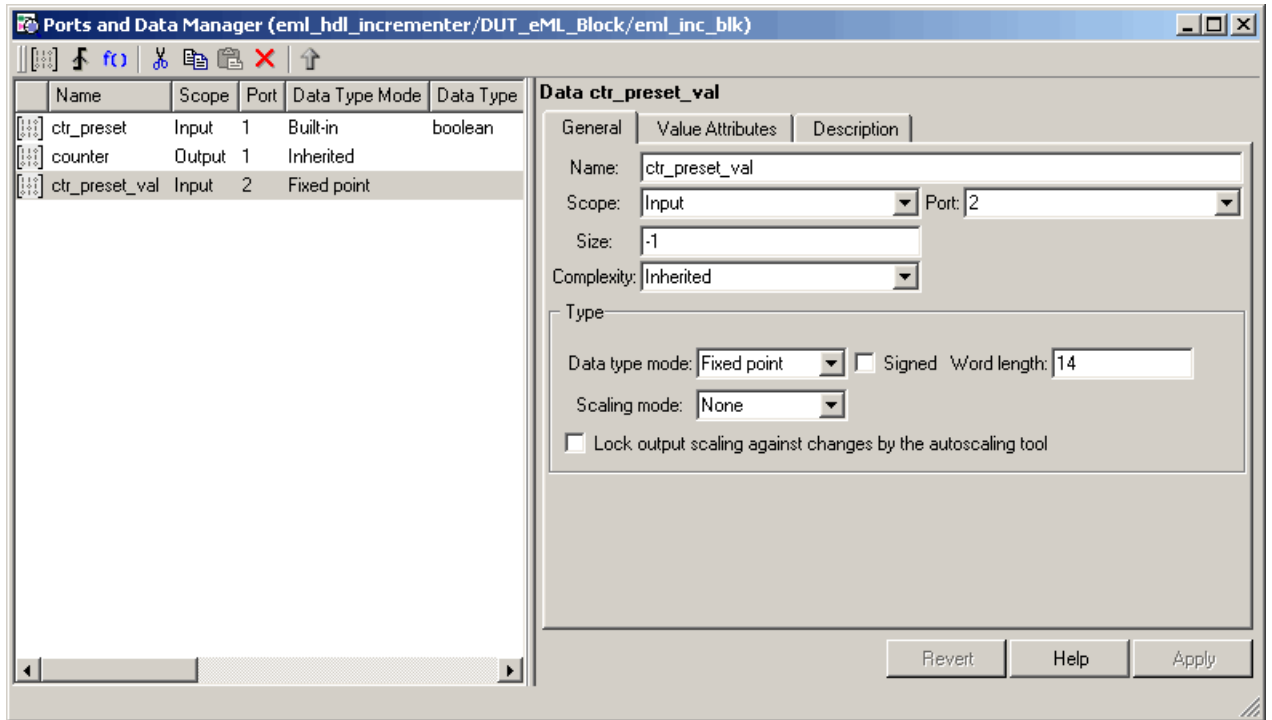


- 2 Double-click the incremter function block, to open the Embedded MATLAB Editor. In the editor window, select **Edit Data Ports** from the **Tools** menu. The Ports and Data Manager dialog box opens.



- 3 Select the `ctr_preset` entry in the port list on the left. Set the **Data type mode** property for this port to `Built-in`. Set the **Data type** property to `boolean`. Click **Apply**.
- 4 Select the `ctr_preset_val` entry in the port list on the left. Set the **Data type mode** property for this port to `Fixed point`. Set the **Word length** property to 14. Click **Apply**.
- 5 Select the `counter` entry in the port list on the left. Verify that the **Data type mode** property for this port is set to `Inherited`. Click **Apply**.

The Ports and Data Manager dialog box should now appear as shown in the following figure.



- 6 Close the Ports and Data Manager dialog box and the Embedded MATLAB Editor.
- 7 Save the model and close the DUT\_eML\_Block subsystem.

## Connecting Subsystem Ports to the Model

Next, connect the ports of the DUT\_eML\_Block subsystem to the model as follows:

- 1 From the Simulink Sources library, add a Constant block to the model. Set the value of the Constant to 1, and the **Output data type mode** to boolean. Change the block label to Preset.
- 2 Make a copy of the Preset Constant block. Set its value to 0, and change its block label to Increment.

- 3** Add a Switch block to the model. Change its label to `Control`. Connect its output to the `In1` port of the `DUT_eML_Block` subsystem.
- 4** From the Simulink Signal Routing library, add a Manual Switch block to the model. Change its label to `Control`. Connect its output to the `In1` port of the `DUT_eML_Block` subsystem.
- 5** Connect the Preset Constant block to the upper input of the `Control` switch block. Connect the Increment Constant block to the lower input of the `Control` switch block.
- 6** Add a third Constant block to the model. Set the value of the Constant to 15, and the **Output data type mode** to `Inherit` via back propagation. Change the block label to `Preset Value`.

Connect the `Preset Value` constant block to the `In2` port of the `DUT_eML_Block` subsystem.

- 7** From the Simulink Sinks library, add a Display block to the model. Connect it to the `Out1` port of the `DUT_eML_Block` subsystem.
- 8** From the Simulink Sinks library, add a To Workspace block to the model. Route the output signal from the `DUT_eML_Block` subsystem to the `To Workspace` block.
- 9** Save the model.

### Checking the Embedded MATLAB Function for Errors

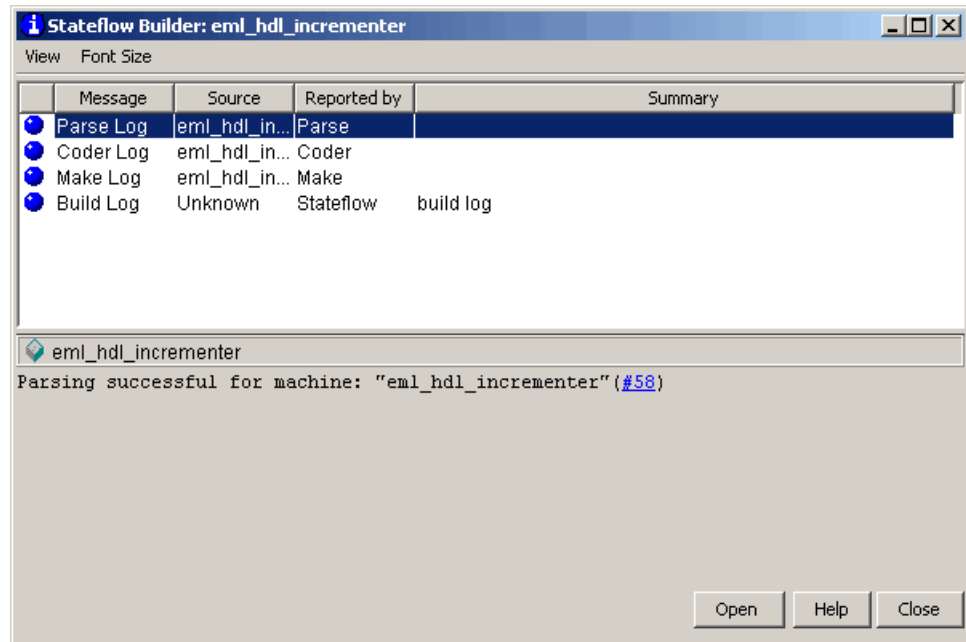
Use the built-in diagnostics of Embedded MATLAB Function blocks to test for syntax errors with the following procedure:

- 1** If it is not already open, open the `eml_hdl_incrementer` model.
- 2** Double-click the Embedded MATLAB Function block `incrementer` to open it for editing.
- 3** In the Embedded MATLAB Editor, select **Build** from the **Tools** menu (or press **CTRL+B**) to compile and build the Embedded MATLAB code.

The build process displays some progress messages. These messages will include some warnings, because the ports of the Embedded MATLAB Function block are not yet connected to any signals. You can ignore these warnings.

The build process builds a C-MEX S-function for use in simulation. The build process includes generation of C code for the S-function. The code generation messages you see during the build process refer to generation of C code, not to HDL code generation.

When the build concludes successfully, a message window is displayed.



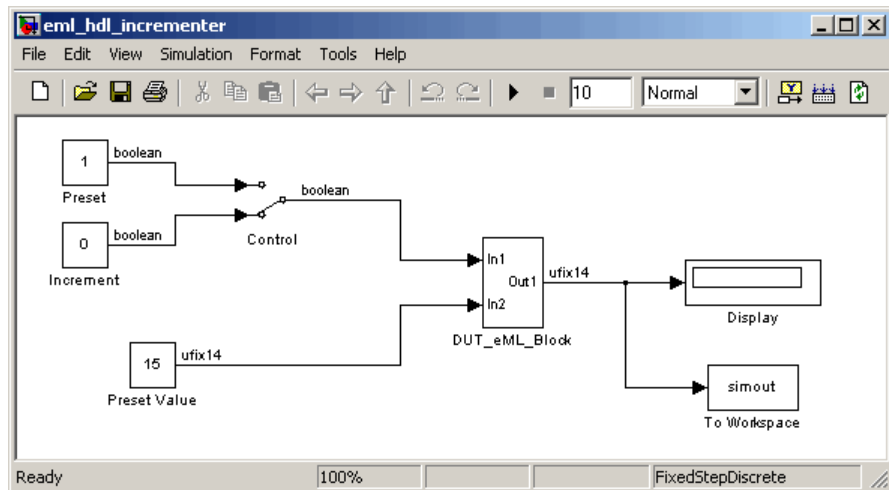
If errors are found, the Diagnostics Manager window lists them. See “Using the Embedded MATLAB Function Block” in the Simulink documentation for information on debugging Embedded MATLAB Function block build errors.



## Compiling the Model and Displaying Port Data Types

In this section you enable the display of port data types and then compile the model. Model compilation verifies that the model structure and settings are correct, and update the model display.

- 1 From the Simulink **Format** menu, select **Port/Signal Displays > Port Data Types**.
- 2 From the Simulink **Edit** menu, select **Update Diagram** (or press **Ctrl+D**) to compile the model. This triggers a rebuild of the embedded MATLAB code. After the model compiles, the block diagram updates to show the port data types. The model should now appear as shown in the following figure.



- 3 Save the model.

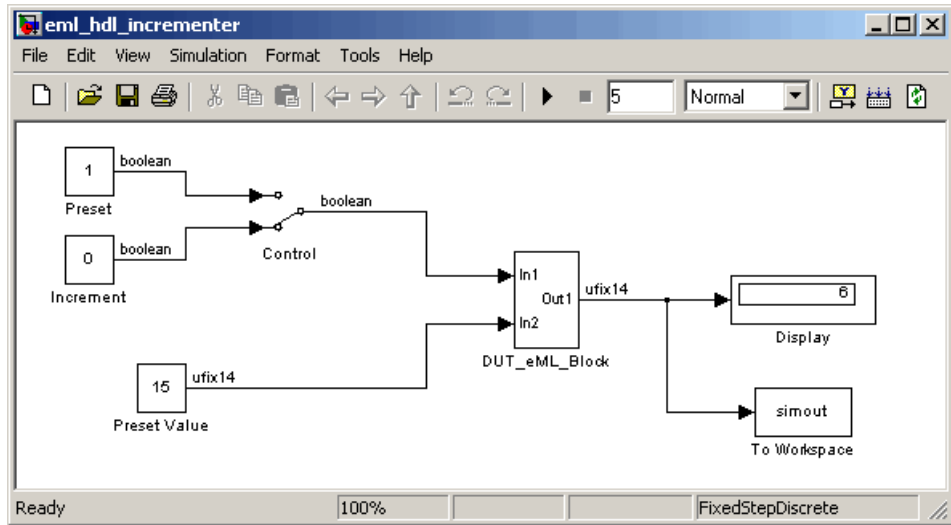
## Simulating the eml\_hdl\_incrementer Model

Click the **Start Simulation** icon to run a simulation.

If necessary, Simulink rebuilds the Embedded MATLAB code before the simulation starts.

After the simulation completes, the Display block shows the final output value returned by the incrementer function block. For example, given a **Start time**

of 0, a **Stop time** of 5, and a zero value presented at the ctr\_preset port, the simulation returns a value of 6, as shown in the following figure.



You may want to experiment with the results of toggling the Control switch, changing the Preset Value constant, and changing the total simulation time. You may also want to examine the workspace variable `simout`, which is bound to the To Workspace block.

## Generating HDL Code

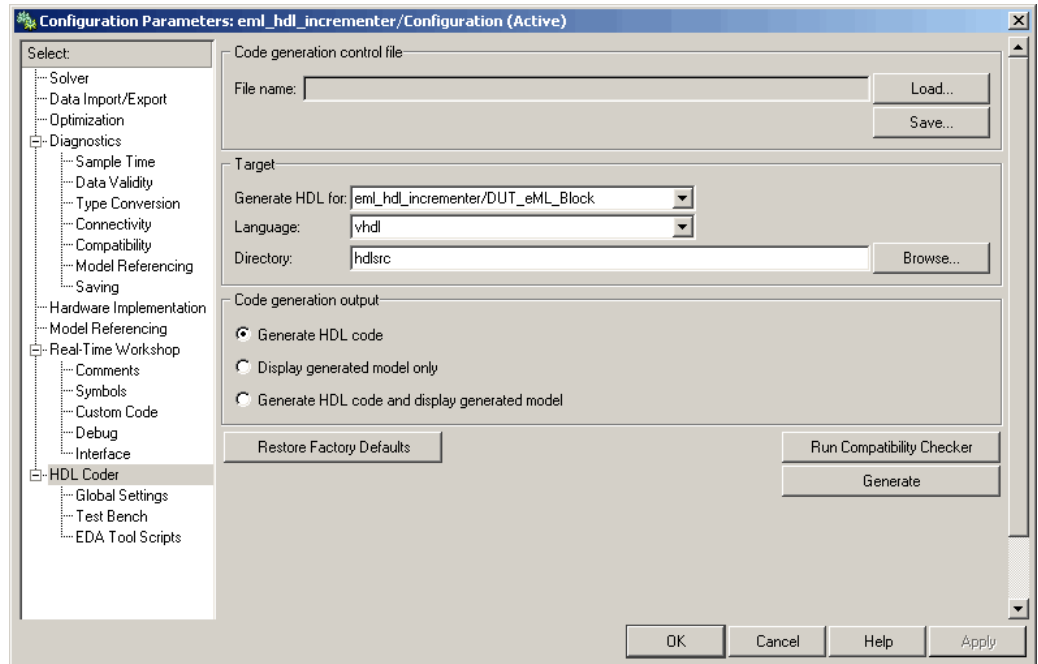
In this section, you select the `DUT_eML_Block` subsystem for HDL code generation, set basic code generation options, and then generate VHDL code for the subsystem.

### Selecting the Subsystem for Code Generation

Select the `DUT_eML_Block` subsystem for code generation, as follows:

- 1 Open the Configuration Parameters dialog box. Click the **HDL Coder** category in the **Select** tree in the left pane of the dialog box.
- 2 Select `eml_hdl_incrementer/DUT_eML_Block` from the **Generate HDL for** menu.

**3** Click **Apply**. The dialog box should now appear as shown in the following figure.



## Generating VHDL Code

The top-level **HDL Coder** options should now be set as follows:

- The **Generate HDL for** field specifies the `em1_hdl_incrementer/DUT_eML_Block` subsystem for code generation.
- The **Language** field specifies (by default) generation of VHDL code.
- The **Directory** field specifies (by default) that the code generation target directory is a subdirectory of your working directory, named `hdlsrc`.

Before generating code, select **Current Directory** from the **Desktop** menu in the MATLAB window. This displays the MATLAB Current Directory

browser, which lets you easily access your working directory and the files that are generated within it.

To generate code:

**1** Click the **Generate** button.

Simulink HDL Coder compiles the model before generating code. Depending on model display options (for example, sample time colors, port data types, etc.), the appearance of the model may change after code generation.

**2** Simulink HDL Coder generates code and displays progress messages. The process should complete successfully with the message

```
### Applying HDL Code Generation Control Statements

### Begin VHDL Code Generation
### Working on em1_hdl_incrementer/DUT_eML_Block as hd1src\DUT_eML_Block.vhd
### Working on em1_hdl_incrementer/DUT_eML_Block/em1_inc_blk as hd1src\em1_inc_blk.vhd
Embedded MATLAB parsing for model "em1_hdl_incrementer"...Done
Embedded MATLAB code generation for model "em1_hdl_incrementer"...Done
### HDL Code Generation Complete.
```

Observe that the names of generated VHDL files in the progress messages are hyperlinked. After code generation completes, you can click these hyperlinks to view the files in the MATLAB editor.

**3** A folder icon for the `hd1src` directory is now visible in the Current Directory browser. To view generated code and script files, double-click the `hd1src` folder icon.

**4** Observe that two VHDL files were generated. The structure of HDL code generated for Embedded MATLAB Function blocks is similar to the structure of code generated for Stateflow charts and Digital Filter blocks. The VHDL files that were generated in the `hd1src` directory are

- `em1_inc_blk.vhd`: VHDL code. This file contains entity and architecture code implementing the actual computations generated for the Embedded MATLAB Function block.

- `DUT_eML_Block.vhd`: VHDL code. This file contains an entity definition and RTL architecture that provide a black box interface to the code generated in `Embedded_MATLAB_Function.vhd`.

The structure of these code files is analogous to the structure of the model, in which the `DUT_eML_Block` subsystem provides an interface between the root model and the incrementer function in the Embedded MATLAB Function block.

The other files that were generated in the `hdlsrc` directory are

- `DUT_eML_Block_compile.do`: ModelSim compilation script (`vcom` command) to compile the VHDL code in the two `.vhd` files.
  - `DUT_eML_Block_synplify.tcl`: Synplify synthesis script.
  - `DUT_eML_Block_map.txt`: Mapping file. This report file maps generated entities (or modules) to the Simulink subsystems that generated them (see “Code Tracing Using the Mapping File” on page 7-6).
- 5** To view the generated VHDL code in the MATLAB editor, double-click the `DUT_eML_Block.vhd` or `eml_inc_blk.vhd` file icons in the Current Directory browser.

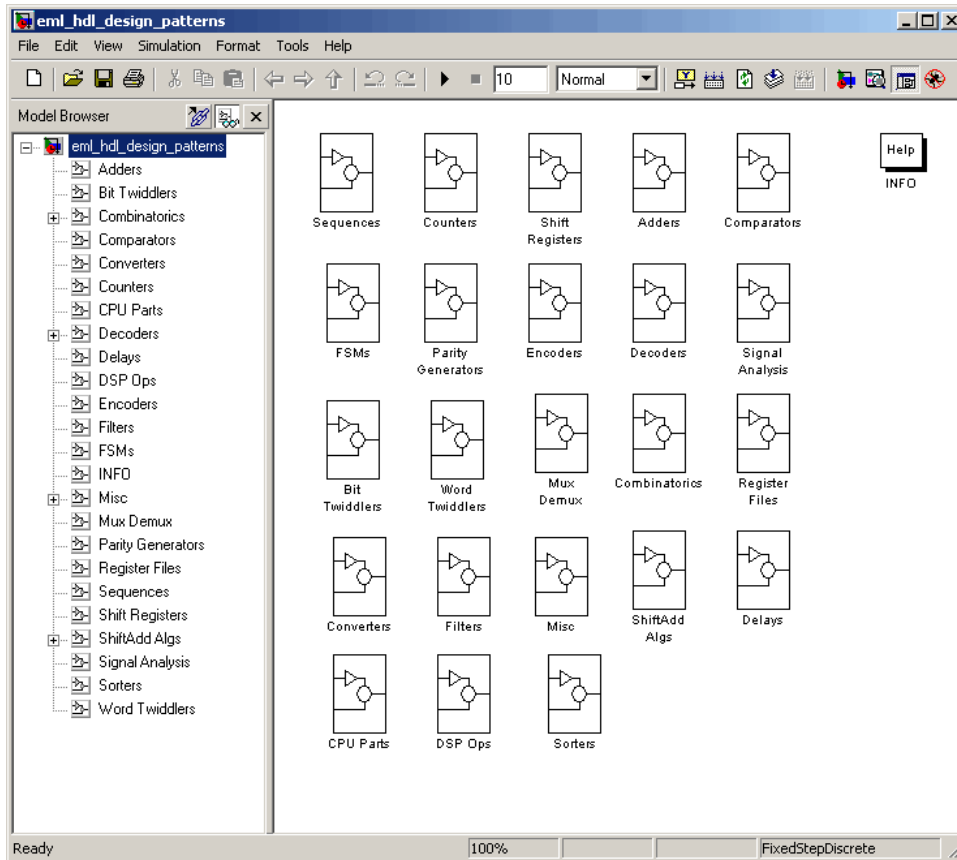
At this point you should study the ENTITY and ARCHITECTURE definitions while referring to “HDL Code Generation Defaults” on page 14-15 in the `makehdl` reference documentation. The reference documentation describes the default naming conventions and correspondences between the elements of a Simulink model (subsystems, ports, signals, etc.) and elements of generated HDL code.

## Useful Embedded MATLAB Design Patterns for HDL

In this section...
“The eml_hdl_design_patterns Library” on page 10-28
“Efficient Fixed-Point Algorithms” on page 10-30
“Using Persistent Variables to Model State” on page 10-34
“Creating Intellectual Property with the Embedded MATLAB Function Block” on page 10-36
“Modeling Control Logic and Simple Finite State Machines” on page 10-36
“Modeling Counters” on page 10-38
“Modeling Hardware Elements” on page 10-40

### The eml\_hdl\_design\_patterns Library

The eml\_hdl\_design\_patterns library is an extensive collection of examples demonstrating useful applications of the Embedded MATLAB Function block in HDL code generation. The following figure shows the library.



The location of the library in the MATLAB directory structure is

```
MATLABROOT\toolbox\hdlcoder\hdlcoderdemos\em1_hdl_design_patterns.mdl
```

Refer to example models in the `em1_hdl_design_patterns` library while reading the following sections. To open the library, type the following command at the MATLAB command prompt:

```
em1_hdl_design_patterns
```

You can use many blocks in the library as cookbook examples of various hardware elements, as follows:

- Copy a block from the library to your model and use it as a computational unit, (generating code in a separate HDL file).
- Copy the code from the block and use it as a subfunction in an existing Embedded MATLAB Function block (generating inline HDL code).

## Efficient Fixed-Point Algorithms

The Embedded MATLAB Function block supports fixed point arithmetic using the Fixed Point Toolbox `fi` function. This function supports several rounding and saturation modes that are useful for coding algorithms that manipulate arbitrary word and fraction lengths in Embedded MATLAB. Supported rounding modes are `ceil`, `fix`, `floor`, and `nearest`. Supported overflow modes are `saturate` and `wrap`.

HDL code generated from the Embedded MATLAB Function block is bit-true to MATLAB semantics. Generated code uses bit manipulation and bit access operators (e.g., `Slice`, `Extend`, `Reduce`, `Concat`, etc.) that are native to VHDL and Verilog.

The following discussion shows how HDL code generated from the Embedded MATLAB Function block follows cast-before-sum semantics, in which addition and subtraction operands are cast to the result type before the addition or subtraction is performed.

Open the `eml_hdl_design_patterns` library and select the `Combinatrics/eml_expr` block. `eml_expr` implements a simple expression containing addition, subtraction, and multiplication operators with differing fixed point data types. The generated HDL code shows the conversion of this expression with fixed point operands. The following listing shows the MATLAB code embedded in the block.

```
% fixpt arithmetic expression
expr = (a*b) - (a+b);

% cast the result to (sfix7_En4) output type
y = fi(expr, 1, 7, 4);
```

The default `fimath` specification for the block determines the behavior of arithmetic expressions using fixed point operands inside the Embedded MATLAB Function block:



```

fimath(...
    'RoundMode', 'ceil',...
    'OverflowMode', 'saturate',...
    'ProductMode', 'FullPrecision', 'ProductWordLength', 32,...
    'SumMode', 'FullPrecision', 'SumWordLength', 32,...
    'CastBeforeSum', true)

```

The data types of operands and output are as follows:

- a: (sfix5\_En2)
- b: (sfix5\_En3)
- y: (sfix7\_En4).

Before HDL Code generation, the operation

```
expr = (a*b) - (a+b);
```

is broken down internally into the following substeps:

```

1 tmul = a * b;
2 tadd = a + b;
3 tsub = tmul - tadd;
4 y = tsub;

```

Based on the fimath settings (see “Recommended Practices” on page 10-53 ) this expression is further broken down internally as follows:

- Based on the specified ProductMode, 'FullPrecision', the output type of tmul is computed as (sfix10\_En5).
- Since the CastBeforeSum property is set to 'true', substep 2 is broken down as follows:

```

t1 = (sfix7_En3) a;
t2 = (sfix7_En3) b;
tadd = t1 + t2;

```

`sfix7_En3` is the result sum type after aligning binary points and accounting for an extra bit to account for possible overflow.

- Based on intermediate types of `tmul` (`sfix10_En5`) and `tadd` (`sfix7_En3`) the result type of the subtraction in substep 3 is computed as `sfix11_En5`. Accordingly, substep 3 is broken down as follows:

```
t3 = (sfix11_En5) tmul;
t4 = (sfix11_En5) tadd;
tsub = t3 - t4;
```

- Finally the result is cast to a smaller type (`sfix7_En4`) leading to the following final expression statements:

```
tmul = a * b;
t1 = (sfix7_En3) a;
t2 = (sfix7_En3) b;
tadd = t1 + t2;
t3 = (sfix11_En5) tmul;
t4 = (sfix11_En5) tadd;
tsub = t3 - t4;
y = (sfix7_En4) tsub;
```

The following listings show the generated VHDL and Verilog code from the `eml_expr` block.

VHDL code excerpt:

```
-- fixpt arithmetic expression
    b_ain := resize(signed(a & '0'), 7);
    b_bin := resize(signed(b), 7);
    a_0 := signed(a) * signed(b);
    ain := resize(a_0, 11);
    b_ain_0 := b_ain + b_bin;
    bin := resize(b_ain_0 & '0' & '0', 11);
    ain_0 := resize(ain, 12);
    bin_0 := resize(bin, 12);
    ain_1 := ain_0 - bin_0;

    IF (ain_1(11) = '0') AND (ain_1(10) /= '0') THEN
        expr := "011111111111";
```

```

ELSIF (ain_1(11) = '1') AND (ain_1(10) /= '1') THEN
    expr := "1000000000";
ELSE
    expr := ain_1(10 DOWNT0 0);
END IF;

-- cast the result to correct output type

IF ((expr(10) = '0') AND (expr(9 DOWNT0 7) /= "000")) OR ((expr(10) = '0')
AND (expr(7 DOWNT0 1) = "0111111")) THEN
    y <= "0111111";
ELSIF (expr(10) = '1') AND (expr(9 DOWNT0 7) /= "111") THEN
    y <= "1000000";
ELSE
    y <= std_logic_vector(expr(7 DOWNT0 1) + ("0" & (expr(0))));
END IF;

```

### Verilog code excerpt:

```

// fixpt arithmetic expression
    b_ain = {a[4], {a, 1'b0}};
    b_bin = b;
    a_0 = a * b;
    ain = a_0;
    b_ain_0 = b_ain + b_bin;
    bin = {{2{b_ain_0[6]}}, {b_ain_0, 2'b00}};
    ain_0 = ain;
    bin_0 = bin;
    ain_1 = ain_0 - bin_0;

    if ((ain_1[11] == 0) && (ain_1[10] != 0))
        expr = 1023;
    else if ((ain_1[11] == 1) && (ain_1[10] != 1))
        expr = -1024;
    else
        expr = ain_1[10:0];

// cast the result to correct output type

    if (((expr[10]== 0)&&(expr[9:7] != 0)) ||((expr[10] == 0) &&(expr[7:1] == 63)))

```

```

        y = 63;
    else if ((expr[10] == 1) && (expr[9:7] != 7))
        y = -64;
    else
        y = expr[7:1] + expr[0];
    end

```

These code excerpts show that the generated HDL code from the Embedded MATLAB Function block represents the bit-true behavior of fixed point arithmetic expressions using high level HDL operators. The HDL code is generated using HDL coding rules like high level `bitselect` and `partselect` replication operators and explicit sign extension and resize operators.

## Using Persistent Variables to Model State

To model complex control logic, the ability to model registers is a basic requirement. In the Embedded MATLAB™ programming model, state-holding elements are represented as persistent variables. A variable that is declared persistent retains its value across function calls in software, and across sample time steps in Simulink. State-holding elements in hardware also require this behavior. Similarly, state-holding elements should retain their values across clock sample times. The values of persistent variables can also be changed using global and local reset conditions.

The subsystem `Delays` in the `eml_hdl_design_patterns` library illustrates how persistent variables can be used to simulate various kinds of delay blocks in Simulink.

The unit `delay` block delays the input sample by one Simulink simulation time step. A persistent variable is used to hold the value, as shown in the following code listing:

```

function y = fcn(u)

persistent u_d;
if isempty(u_d)
    u_d = fi(-1, numerictype(u), fimath(u));
end

```

```

% return delayed input from last sample time hit
y = u_d;

% store the current input to be used later
u_d = u;

```

In this example, `u` is a fixed-point operand of type `sfix6`. In the generated HDL code, initialization of persistent variables is moved into the master reset region in the initialization process as follows.

```

ENTITY unit_delay IS
  PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    u : IN std_logic_vector(5 DOWNT0 0);
    y : OUT std_logic_vector(5 DOWNT0 0));
END unit_delay;

ARCHITECTURE fsm_SFHDL OF unit_delay IS

  SIGNAL u_d : signed(5 DOWNT0 0);
  SIGNAL u_d_next : signed(5 DOWNT0 0);

BEGIN
  initialize_unit_delay : PROCESS (reset, clk)
    -- local variables
  BEGIN
    IF reset = '1' THEN
      u_d <= to_signed(-8, 6);
    ELSIF clk'EVENT AND clk= '1' THEN
      IF clk_enable= '1' THEN
        u_d <= u_d_next;
      END IF;
    END IF;
  END PROCESS initialize_unit_delay;

```

Refer to the Delays subsystem to see how vectors of persistent variables can be used to model integer delay, tap delay, and tap delay vector blocks.

These design patterns are useful in implementing sequential algorithms that carry state between invocations of the Embedded MATLAB block in a Simulink model.

## **Creating Intellectual Property with the Embedded MATLAB Function Block**

The Embedded MATLAB Function block lets you quickly author intellectual property (IP). It also lets you rapidly create alternate implementations of a part of an algorithm.

For example, the subsystem Comparators in the `eml_hdl_design_patterns` library includes several alternate algorithms for finding the minimum value of a vector. The `Comparators/eml_linear_min` block finds the minimum of the vector in a linear mode serially. The `Comparators/eml_tree_min` block compares the elements in a tree structure. The tree implementation can achieve a higher clock frequency by adding pipeline registers between the  $\log_2(N)$  stages. (See `eml_hdl_design_patterns/Filters` for an example.)

Now consider replacing the simple comparison operation in the Comparators blocks with an arithmetic operation (e.g., addition, subtraction, or multiplication) where intermediate results must be quantized. Using `fimath` rounding settings, you can fine tune intermediate value computations before intermediate values feed into the next stage. This can be a powerful technique for tuning the generated hardware or customizing your algorithm.

By using Embedded MATLAB Function blocks in this way, you can guide the detailed operation of the HDL code generator even while writing high-level algorithms.

## **Modeling Control Logic and Simple Finite State Machines**

Embedded MATLAB control constructs such as `switch/case` and `if-elseif-else`, coupled with fixed point arithmetic operations, let you model control logic quickly.

The FSMs/mealy\_fsm\_blk and FSMs/moore\_fsm\_blk blocks in the eml\_hdl\_design\_patterns library provide example implementations of Mealy and Moore finite state machines in Embedded MATLAB.

The following listing implements a Moore state machine.

```
function Z = moore_fsm(A)

persistent moore_state_reg;
if isempty(moore_state_reg)
    moore_state_reg = fi(0, 0, 2, 0);
end

S1 = 0;
S2 = 1;
S3 = 2;
S4 = 3;

switch uint8(moore_state_reg)

case S1,
    Z = true;
    if (~A)
        moore_state_reg(1) = S1;
    else
        moore_state_reg(1) = S2;
    end
case S2,
    Z = false;
    if (~A)
        moore_state_reg(1) = S1;
    else
        moore_state_reg(1) = S2;
    end
case S3,
    Z = false;
    if (~A)
        moore_state_reg(1) = S2;
    else
        moore_state_reg(1) = S3;
    end
```

```
        end
    case S4,
        Z = true;
        if (~A)
            moore_state_reg(1) = S1;
        else
            moore_state_reg(1) = S3;
        end
    otherwise,
        Z = false;
end
```

In this example, a persistent variable (`moore_state_reg`) models state variables. The output depends only on the state variables, thus modeling a Moore machine.

The FSMs/`mealy_fsm_blk` block in the `eml_hdl_design_patterns` library implements a Mealy state machine. A Mealy state machine differs from a Moore state machine in that the outputs depend on inputs as well as state variables.

Simple state machines and other control-based hardware algorithms, such as pattern matchers, or synchronization-related controllers, can be quickly modeled using control statements and persistent variables in Embedded MATLAB.

For modeling more complex and hierarchical state machines with complicated temporal logic, use Stateflow to model the state machine.

## Modeling Counters

To implement arithmetic and control logic algorithms in Embedded MATLAB Function blocks intended for HDL code generation, there are some simple HDL related coding requirements:

- The top level Embedded MATLAB Function block must be called once per time step.
- It must be possible to fully unroll program loops.



- Persistent variables with proper reset values and update logic must be used to hold values across Simulink time steps.
- Quantized data variables must be used inside loops.

The following script shows how to model a synchronous up/down counter with preset values and control inputs. The example provides both master reset control of persistent state variables and local reset control using block inputs (e.g. `presetClear`). The `isempty` condition enters the initialization process under the control of a synchronous reset. The `presetClear` section is implemented in the output section in the generated HDL code.

Both the up and down case statements implementing the count loop require that the values of the counter are quantized after addition or subtraction. By default, Embedded MATLAB automatically propagates fixed-point settings specified for the block. In this script, however, fixed-point settings for intermediate quantities and constants are explicitly specified.

```
function [Q, QN] = up_down_ctr(upDown, presetClear, loadData, presetData)

% up down result
% 'result' synthesizes into sequential element

result_nt = numerictype(0,4,0);
result_fm = fimath('OverflowMode', 'saturate', 'RoundMode', 'floor');

initVal = fi(0, result_nt, result_fm);

persistent count;
if isempty(count)
    count = initVal;
end

if presetClear
    count = initVal;
elseif loadData
    count = presetData;
elseif upDown
    inc = count + fi(1, result_nt, result_fm);
    -- quantization of output
```

```
        count = fi(inc, result_nt, result_fm);
    else
        dec = count - fi(1, result_nt, result_fm);
        -- quantization of output
        count = fi(dec, result_nt, result_fm);
    end

    Q = count;
    QN = bitcmp(count);
```

## Modeling Hardware Elements

The following code example shows how to model shift registers in Embedded MATLAB by using the `bitsliceget` and `bitconcat` function. This function implements a serial input and output shifters with a 32-bit fixed-point operand input. See the Shift Registers/`shift_reg_1by32` block in the `eml_hdl_design_patterns` library for more details.

```
function sr_out = fcn(shift, sr_in)
%shift register 1 by 32

persistent sr;
if isempty(sr)
    sr = fi(0, 0, 32, 0, 'fimath', fimath(sr_in));
end

% return sr[31]
sr_out = getmsb(sr);

if (shift)
    % sr_new[32:1] = sr[31:1] & sr_in
    sr = bitconcat(bitsliceget(sr, 31, 1), sr_in);
end
```

The following code example shows VHDL process code generated for the `shift_reg_1by32` block.

```
shift_reg_1by32 : PROCESS (sr, shift, sr_in)
    -- local variables
BEGIN
```

```
sr_next <= sr;
--shift register 1 by 32
-- return sr[31]
sr_out <= sr(31);

IF shift /= '0' THEN
    -- sr_new[32:1] = sr[31:1] & sr_in
    sr_next <= sr(30 DOWNT0 0) & sr_in;
END IF;

END PROCESS shift_reg_1by32;
```

The Shift Registers/shift\_reg\_1by64 block shows a 64 bit shifter. In this case, the shifter uses two fixed point words, to represent the operand, overcoming the 32-bit word length limitation for fixed-point integers.

Browse the `eml_hdl_incrementer` model for other useful hardware elements that can be easily implemented using Embedded MATLAB.

## Using Fixed Point Bitwise Functions

### In this section...

“Overview” on page 10-42

“Bitwise Functions Supported for HDL Code Generation” on page 10-42

“Bit Slice and Bit Concatenation Functions” on page 10-48

“Shift and Rotate Functions” on page 10-49

### Overview

Embedded MATLAB supports many bitwise functions that operate on fixed-point integers of arbitrary length. For general information on Embedded MATLAB bitwise functions, see “Bitwise Functions” in the Fixed-Point Toolbox documentation.

This section describes Simulink HDL Coder support for HDL code generation for these functions. “Bitwise Functions Supported for HDL Code Generation” on page 10-42 summarizes the supported functions, with notes that describe considerations specific to HDL code generation. “Bit Slice and Bit Concatenation Functions” on page 10-48 and “Shift and Rotate Functions” on page 10-49 provide usage examples, with corresponding Embedded MATLAB and generated HDL code.

The Bit Twiddlers/hdl\_bit\_ops block in the eml\_hdl\_design\_patterns library provides further examples of how to use these functions for various bit manipulation operations.

### Bitwise Functions Supported for HDL Code Generation

The following table summarizes Embedded MATLAB bitwise functions that are supported for HDL code generation. The Description column notes considerations that are specific to HDL. The following conventions are used in the table:

- *a, b*: Denote fixed-point integer operands.
- *idx*: Denotes an index to a bit within an operand. Indexes can be scalar or vector, depending on the function.

Embedded MATLAB functions follow the MATLAB (1-based) indexing conventions. In generated HDL code, such indexes are converted to zero-based indexing conventions.

- `lidx`, `ridx`: denote indexes to the left and right boundaries delimiting bit fields. Indexes can be scalar or vector, depending on the function.
- `val`: Denotes a Boolean value.

---

**Note** Indexes, operands, and values passed as arguments bitwise functions can be scalar or vector, depending on the function. See “Bitwise Functions” in the Fixed-Point Toolbox documentation for information on the individual functions.

---

Embedded MATLAB Function Syntax	Description	See Also
<code>bitand(a, b)</code>	Bitwise AND	<code>bitand</code>
<code>bitandreduce(a, lidx, ridx)</code>	Bitwise AND of a field of consecutive bits within <code>a</code> . The field is delimited by <code>lidx</code> , <code>ridx</code> .  Output data type: <code>ufix1</code>  For VHDL, generates the bitwise AND operator operating on a set of individual slices  For Verilog, generates the reduce operator:  $\&a[lidx:ridx]$	<code>bitandreduce</code>
<code>bitcmp(a)</code>	Bitwise complement	<code>bitcmp</code>

<b>Embedded MATLAB Function Syntax</b>	<b>Description</b>	<b>See Also</b>
bitconcat(a, b)	<p>Concatenate two fixed-point operands.</p> <p>Operands can be of different signs.</p> <p>Output data type: <code>ufixN</code>, where N is the sum of the word lengths of a and b.</p> <p>For VHDL, generates the concatenation operator: <code>(a &amp; b)</code></p> <p>For Verilog, generates the concatenation operator: <code>{a , b}</code></p>	bitconcat
bitget(a,idx)	<p>Access a bit at position <code>idx</code>.</p> <p>For VHDL, generates the slice operator: <code>a(idx)</code></p> <p>For Verilog, generates the slice operator: <code>a[idx]</code></p>	bitget
bitor(a, b)	Bitwise OR	bitor
bitorreduce(a, lidx, ridx)	<p>Bitwise OR of a field of consecutive bits within a. The field is delimited by <code>lidx</code> and <code>ridx</code>.</p> <p>Output data type: <code>ufix1</code></p> <p>For VHDL, generates the bitwise OR operator operating on a set of individual slices.</p> <p>For Verilog, generates the reduce operator:</p> <p style="text-align: center;"><code> a[lidx:ridx]</code></p>	bitorreduce

<b>Embedded MATLAB Function Syntax</b>	<b>Description</b>	<b>See Also</b>
bitrol(a, idx)	<p>Rotate left.</p> <p>idx must be a positive integer. The value of idx can be greater than the word length of a. idx is always normalized to <math>\text{mod}(\text{idx}, \text{wlen})</math>, where wlen is the word length of a.</p> <p>For VHDL, generates the rol operator.</p> <p>For Verilog, generates the following expression where w1 is the word length of a:</p> $a \ll \text{idx} \mid\mid a \gg \text{w1} - \text{idx}$	bitrol
bitror(a, idx)	<p>Rotate right.</p> <p>idx must be a positive integer. The value of idx can be greater than the word length of a. idx is always normalized to <math>\text{mod}(\text{idx}, \text{wlen})</math>, where wlen is the word length of a.</p> <p>For VHDL, generates the ror operator.</p> <p>For Verilog, generates the following expression (where w1 is the word length of a:</p> $a \gg \text{idx} \mid\mid a \ll \text{w1} - \text{idx}$	bitror
bitset(a, idx, val)	<p>Set or clear bit(s) at position idx.</p> <p>If val = 0, clears the indicated bit(s). Otherwise, sets the indicated bits.</p>	bitset

<b>Embedded MATLAB Function Syntax</b>	<b>Description</b>	<b>See Also</b>
bitshift(a, idx)	<p><i>Note: for efficient HDL code generation use, use bitsll, bitsrl, or bitsra instead of bitshift.</i></p> <p>Shift left or right, based on the positive or negative integer value of idx.</p> <p>idx must be an integer.</p> <p>For positive values of idx, shift left idx bits.</p> <p>For negative values of idx, shift right idx bits.</p> <p>If idx is a variable, generated code contains logic for both left shift and right shift.</p> <p>Result values saturate if the overflowMode of a is set to saturate.</p>	bitshift
bitsliceget(a, lidx, ridx)	<p>Access consecutive set of bits from lidx to ridx.</p> <p>Output data type: ufixN, where N = lidx-ridx+1.</p>	bitsliceget
bitsll(a, idx)	<p>Shift left logical.</p> <p>idx must be a scalar within the range</p> $0 \leq \text{idx} < w1$ <p>where w1 is the word length of a.</p> <p>Overflow and rounding modes of input operand a are ignored.</p> <p>Generates sll operator in VHDL.</p> <p>Generates &lt;&lt; operator in Verilog.</p>	bitsll



<b>Embedded MATLAB Function Syntax</b>	<b>Description</b>	<b>See Also</b>
bitsra(a, idx)	Shift right arithmetic. idx must be a scalar within the range $0 \leq \text{idx} < w1$ where w1 is the word length of a, Overflow and rounding modes of input operand a are ignored. Generates sra operator in VHDL. Generates >>> operator in Verilog.	bitsra
bitsrl(a, idx)	Shift right logical. idx must be a scalar within the range $0 \leq \text{idx} < w1$ where w1 is the word length of a. Overflow and rounding modes of input operand a are ignored. Generates srl operator in VHDL. Generates >> operator in Verilog.	bitsrl
bitxor(a, b)	Bitwise XOR	bitxor
bitxorreduce(a, lidx, ridx)	Bitwise XOR reduction. Bitwise XOR of a field of consecutive bits within a. The field is delimited by lidx and ridx. Output data type: ufix1 For VHDL, generates a set of individual slices. For Verilog, generates the reduce operator: $\wedge a[\text{lidx}:\text{ridx}]$	bitxorreduce

<b>Embedded MATLAB Function Syntax</b>	<b>Description</b>	<b>See Also</b>
getlsb(a)	Return value of LSB.	getlsb
getmsb(a)	Return value of MSB.	getmsb

### Bit Slice and Bit Concatenation Functions

This section shows you how to use the Embedded MATLAB `bitsliceget` and `bitconcat` functions to access and manipulate bit slices (fields) in a fixed-point or integer word. As an example, consider the operation of swapping the upper and lower 4-bit nibbles of an 8-bit byte. The following example accomplishes this without resorting to traditional mask-and-shift techniques.

```
function y = fcn(u)
% NIBBLE SWAP
y = bitconcat(
    bitsliceget(u, 4, 1),
    bitsliceget(u, 8, 5));
```

The `bitsliceget` and `bitconcat` functions map directly to slice and concat operators in both VHDL and Verilog.

The following listing shows the corresponding VHDL code generated by Simulink HDL Coder.

```
ENTITY fcn IS
    PORT (
        clk : IN std_logic;
        clk_enable : IN std_logic;
        reset : IN std_logic;
        u : IN std_logic_vector(7 DOWNTO 0);
        y : OUT std_logic_vector(7 DOWNTO 0));
END nibble_swap_7b;

ARCHITECTURE fsm_SFHDL OF fcn IS
```

```

BEGIN
  -- NIBBLE SWAP
  y <= u(3 DOWNT0 0) & u(7 DOWNT0 4);
END fsm_SFHDL;

```

The following listing shows the corresponding Verilog code generated by Simulink HDL Coder.

```

module fcn (clk, clk_enable, reset, u, y );
  input clk;
  input clk_enable;
  input reset;
  input [7:0] u;
  output [7:0] y;

  // NIBBLE SWAP
  assign y = {u[3:0], u[7:4]};

endmodule

```

## Shift and Rotate Functions

The Embedded MATLAB shift and rotate functions mimic HDL-specific operators without saturation and rounding logic.

The following Embedded MATLAB function implements a barrel shifter/rotator that performs a selected operation (based on the mode argument) on a fixed point input operand.

```

function y = fcn(u, mode)
% Multi Function Barrel Shifter/Rotator

% fixed width shift operation
fixed_width = uint8(3);

switch mode
  case 1
    % shift left logical
    y = bitsll(u, fixed_width);
  case 2

```

```
        % shift right logical
        y = bitsrl(u, fixed_width);
    case 3
        % shift right arithmetic
        y = bitsra(u, fixed_width);
    case 4
        % rotate left
        y = bitrol(u, fixed_width);
    case 5
        % rotate right
        y = bitror(u, fixed_width);
    otherwise
        % do nothing
        y = u;
end
```

In VHDL code generated for this function, the shift and rotate functions map directly to shift and rotate instructions in VHDL.

```
CASE mode IS
    WHEN "00000001" =>
        -- shift left logical
        cr := signed(u) sll 3;
        y <= std_logic_vector(cr);
    WHEN "00000010" =>
        -- shift right logical
        b_cr := signed(u) srl 3;
        y <= std_logic_vector(b_cr);
    WHEN "00000011" =>
        -- shift right arithmetic
        c_cr := SHIFT_RIGHT(signed(u) , 3);
        y <= std_logic_vector(c_cr);
    WHEN "00000100" =>
        -- rotate left
        d_cr := signed(u) rol 3;
        y <= std_logic_vector(d_cr);
    WHEN "00000101" =>
        -- rotate right
        e_cr := signed(u) ror 3;
        y <= std_logic_vector(e_cr);
```

```

        WHEN OTHERS =>
            -- do nothing
            y <= u;
        END CASE;

```

The corresponding Verilog code is similar, except that Verilog does not have native operators for rotate instructions.

```

case ( mode)
1 :
    begin
        // shift left logical
        cr = u <<< 3;
        y = cr;
    end
2 :
    begin
        // shift right logical
        b_cr = u >> 3;
        y = b_cr;
    end
3 :
    begin
        // shift right arithmetic
        c_cr = u >>> 3;
        y = c_cr;
    end
4 :
    begin
        // rotate left
        d_cr = (u <<< 3) | (u >> 3);
        y = d_cr;
    end
5 :
    begin
        // rotate right
        e_cr = (u >> 3) | (u <<< 3);
        y = e_cr;
    end
default :

```

```
        begin
            // do nothing
            y = u;
        end
    endcase
```

## Recommended Practices

### In this section...

“Introduction” on page 10-53

“Build the Embedded MATLAB Code First” on page 10-53

“Use Optimal FIMATH Settings” on page 10-53

“Use Optimal Fixed Point Option Settings” on page 10-54

### Introduction

This section describes recommended practices when using the Embedded MATLAB Function block for HDL code generation.

The MathWorks strongly recommends that you set Embedded MATLAB Function block options as described in this section. By using these settings, you can significantly increase the efficiency of generated HDL code. See “Setting Optimal Fixed Point Options for the Embedded MATLAB Function Block” on page 10-12 for an example.

### Build the Embedded MATLAB Code First

Before generating HDL code for a subsystem containing an Embedded MATLAB Function block, it is strongly recommended that you build the Embedded MATLAB code to check for errors. To build the code, select **Build** from the **Tools** menu in the Embedded MATLAB editor (or press **CTRL+B**).

### Use Optimal FIMATH Settings

Use the default FIMATH specification, but change the following properties:

- ProductMode property of the FIMATH specification: set to 'FullPrecision'
- SumMode property of the FIMATH specification: set to 'FullPrecision'

The following listing shows the resultant FIMATH setting.

```
fimath(...  
    'RoundMode', 'floor',...
```

```
'OverflowMode', 'wrap',...  
'ProductMode', 'FullPrecision', 'ProductWordLength', 32,...  
'SumMode', 'FullPrecision', 'SumWordLength', 32,...  
'CastBeforeSum', true)
```

---

**Note** When the FIMATH OverflowMode property of the FIMATH specification is set to 'Saturate', HDL code generation is disallowed for the following cases:

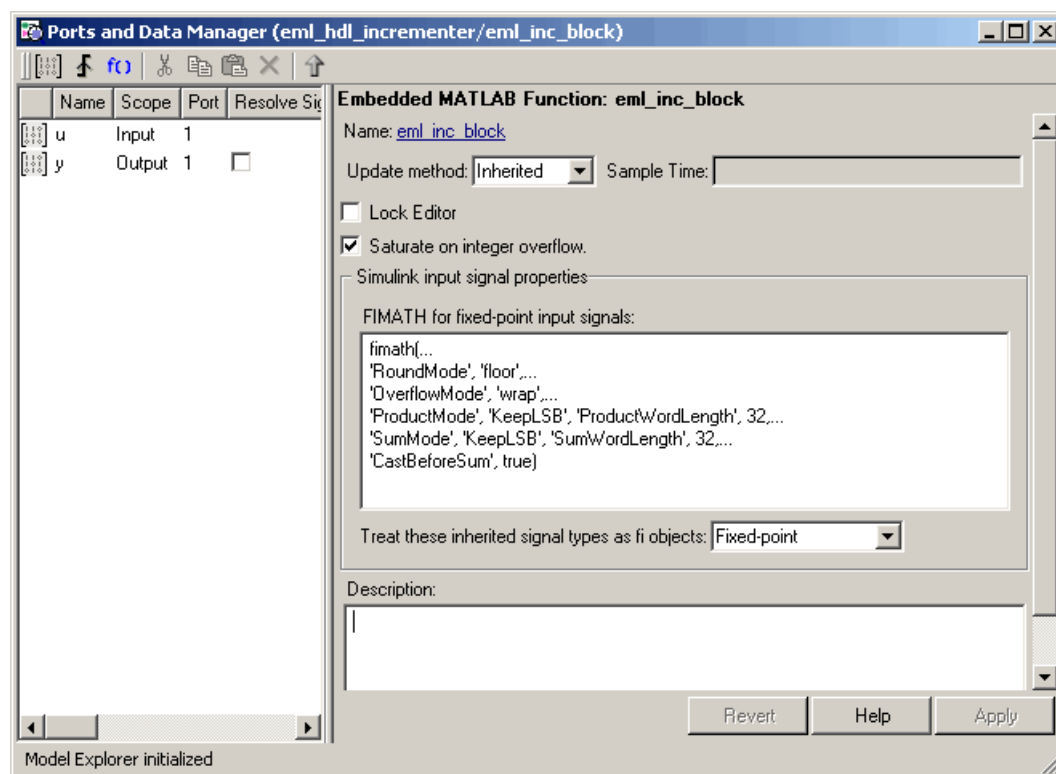
- SumMode is set to 'SpecifyPrecision'
- ProductMode is set to 'SpecifyPrecision'

---

### Use Optimal Fixed Point Option Settings

Use the default (Fixed-point) setting for the **Treat these inherited signal types as fi objects** option, as shown in the following figure.





## Language Support

### In this section...

“Fixed-Point Embedded MATLAB Runtime Library Support” on page 10-56

“Variables and Constants” on page 10-57

“Arithmetic Operators” on page 10-61

“Relational Operators” on page 10-62

“Logical Operators” on page 10-63

“Control Flow Statements” on page 10-63

## Fixed-Point Embedded MATLAB Runtime Library Support

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder supports most of the fixed-point runtime library functions supported by Embedded MATLAB. For a complete list of these functions, see “Supported Functions and Limitations of Fixed-Point Embedded MATLAB™” in the Fixed Point Toolbox documentation.

Some functions are not supported, or are subject to some restrictions. These functions are summarized in the following table.

Function	Restriction	Notes
complex	Not supported	Complex data types are not supported in this release.
conj	Not supported	Complex data types are not supported in this release.
ctranspose	Not supported	Complex data types are not supported in this release.
disp	Not supported	

<b>Function</b>	<b>Restriction</b>	<b>Notes</b>
get	Not supported	This function returns a struct. Struct data types are not supported in this release.
imag	Not supported	Complex data types are not supported in this release.
pow2	Not supported	
real	Not supported	
divide	Supported, with restrictions	The divisor must be a constant and a power of two.
fi	Supported, with restrictions	Only the following rounding modes are supported: <code>ceil</code> , <code>fix</code> , <code>floor</code> , <code>nearest</code> .
fimath	Supported, with restrictions	Only the following rounding modes are supported: <code>ceil</code> , <code>fix</code> , <code>floor</code> , <code>nearest</code> .
subsasgn	Supported, with restrictions	Subscripted assignment supported; see “Data Type Usage” on page 10-58
subsref	Supported, with restrictions	Subscripted reference supported; see “Data Type Usage” on page 10-58

## Variables and Constants

This section summarizes supported data types and typing rules for variable and constants, and the use of persistent variables in modeling registers.

### Data Type Usage

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder supports a subset of MATLAB data types. The following table summarizes supported and unsupported data types.

Type(s)	Support	Notes
Integer	Supported: <ul style="list-style-type: none"> <li>• uint8, uint16, uint32,</li> <li>• int8, int16, int32</li> </ul>	
Real	Supported: <ul style="list-style-type: none"> <li>• double</li> <li>• single</li> </ul>	HDL code generated with double or single data types is not synthesizable.
Character	Supported: <ul style="list-style-type: none"> <li>• char</li> </ul>	
Logical	Supported: <ul style="list-style-type: none"> <li>• Boolean</li> </ul>	
Fixed point	Supported: <ul style="list-style-type: none"> <li>• Scaled (binary point only) fixed point numbers</li> <li>• Custom integers (zero binary point)</li> </ul>	<p>Fixed point numbers with slope (not equal to 1.0) and bias (not equal to 0.0) are not supported.</p> <p>Maximum word size for fixed-point numbers is 32 bits.</p> <p>The convergent and matlab rounding modes are not currently supported. Do not specify these modes in fimath in specifications.</p>
Vectors	Supported: <ul style="list-style-type: none"> <li>• unordered {N}</li> <li>• row {1, N}</li> <li>• column {N, 1}</li> </ul>	<p>The maximum number of vector elements allowed is <math>2^{32}</math>.</p> <p>Embedded MATLAB requires a variable to be fully defined before it is subscripted.</p>

Type(s)	Support	Notes
Matrix	N/A	Matrices are not supported in the current release.
Complex	N/A	Complex data types are not supported in the current release.
Struct	N/A	Struct data types are not supported in the current release.
Cell arrays	N/A	Cell arrays are not supported in the current release.

## Typing Ports, Variables and Constants

Strong typing rules are applied to Embedded MATLAB Function blocks, as follows:

- All input and output port data types must be resolved at model compilation time.
  - If the data type of an input port is unspecified when the model is compiled, the port is assigned the data type of the signal driving the port.
  - If the data type of an output port is unspecified when the model is compiled, the output port type is determined by the first assignment to the output variable.
- Similarly, all constant literals are strongly typed. If you do not specify the data type of a constant explicitly, its type is determined by internal rules. To specify the data type of a constant, use cast functions (e.g., `uint8`, `uint16`, etc.) or `fi` functions using `fimath` specifications.
- After you have defined a variable, do not change its data type. Variable types cannot be changed dynamically by assigning a different value as in MATLAB. Dynamic typing will lead to a compile time error.
- After you have defined a variable, do not change its size. Variables cannot be grown or resized dynamically.
- Do not use output variables to model registered output; in Embedded MATLAB, outputs are never persistent. Use persistent variables for this purpose, as described in “Persistent Variables” on page 10-60.

## Persistent Variables

Persistent variables let you model registers. If you need to preserve state between invocations of an Embedded MATLAB Function block, use persistent variables.

Each persistent variable must be initialized with a statement specifying its size and type before it is referenced. You can initialize a persistent variable with either a constant value or a variable, as in the following code listings:

```
% Initialize with a constant
persistent p;
if isempty(p)
    p = fi(0,0,8,0);
end

% Initialize with a variable
initval = fi(0,0,8,0);

persistent p;
if isempty(p)
    p = initval;
end
```

When testing whether a persistent variable has been initialized, it is good practice to use simple logical expressions, as in the preceding examples. Using simple expressions ensures that the HDL code for the test is generated in the reset process, and therefore is executed only once.

You can initialize multiple variables based on a single simple logical expression, as in the following example:

```
% Initialize with variables
initval1 = fi(0,0,8,0);
initval2 = fi(0,0,7,0);

persistent p;
if isempty(p)
    x = initval1;
    y = initval2;
end
```

See also “The Incrementer Function Code” on page 10-8 for an example of the initialization and use of a persistent variable.

---

**Note** If persistent variables are not initialized properly, unnecessary sentinel variables can appear in the generated code.

---

**Limitation on Use of Persistent Variables.** As described in “Using Persistent Variables to Model State” on page 10-34, you can use persistent variables in Embedded MATLAB code to simulate various kinds of Simulink delay blocks.

However, note that Simulink sees the ports on the Embedded MATLAB block as direct feedthrough ports, and does not recognize delay constructs internal to the Embedded MATLAB block. Therefore a feedback loop in the model causes an algebraic loop condition in Simulink.

To work around this limitation:

- Keep the combinatorial logic inside the Embedded MATLAB block for one of the blocks in the loop which has a persistent variable for the output or input. Remove the persistent variable.
- Place a Simulink Unit Delay external to the Embedded MATLAB block.

## Arithmetic Operators

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder supports the arithmetic operators (and their M function equivalents) listed in the following table.

Operation	Operator Syntax	M Function Equivalent	Fixed Point Support?
Binary addition	A+B	plus(A,B)	Y
Matrix Multiplication	A*B	mtimes(A,B)	Y
Arraywise multiplication	A.*B	times(A,B)	Y
Matrix right division	A/B	mrdivide(A,B)	Y

Operation	Operator Syntax	M Function Equivalent	Fixed Point Support?
Arraywise right division	A ./B	rdivide(A,B)	Y
Matrix left division	A \B	mldivide(A,B)	Y
Arraywise left division	A ./B	ldivide(A,B)	Y
Matrix power	A^B	mpower(A,B)	Y
Arraywise power	A.^B	power(A,B)	Y
Complex transpose	A'	ctranspose(A)	Y
Matrix transpose	A.'	transpose(A)	Y
Matrix concat	[A B]	None	Y
Matrix index <i>Note:</i> Embedded MATLAB requires a variable to be fully defined before it is subscripted.	A(r c)	None	Y.

## Relational Operators

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder supports the relational operators (and their M function equivalents) listed in the following table.

Relation	Operator Syntax	M Function Equivalent	Fixed Point Support?
Less than	A<B	lt(A,B)	Y
Less than or equal to	A<=B	le(A,B)	Y
Greater than or equal to	A>=B	ge(A,B)	Y
Greater than	A>B	gt(A,B)	Y



Relation	Operator Syntax	M Function Equivalent	Fixed Point Support?
Equal	A==B	eq(A,B)	Y
Not Equal	A~=B	ne(A,B)	Y

## Logical Operators

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder supports the logical operators (and their M function equivalents) listed in the following table.

Relation	Operator Syntax	M Function Equivalent	Fixed Point Support?	Notes
Logical And	A&B	and(A,B)	Y	
Logical Or	A B	or(A,B)	Y	
Logical Xor	A xor B	xor(A,B)	Y	
Logical And (short circuiting)	A&&B	N/A	Y	Use short circuiting logical operators within conditionals. See also “Control Flow Statements” on page 10-63.
Logical Or (short circuiting)	A  B	N/A	Y	Use short circuiting logical operators within conditionals. See also “Control Flow Statements” on page 10-63.
Element complement	~A	not(A)	Y	

## Control Flow Statements

When generating code for the Embedded MATLAB Function block, Simulink HDL Coder imposes some restrictions on the use of control flow statements and constructs. The following table summarizes supported and unsupported control flow statements.

<b>Control Flow Statement</b>	<b>Notes</b>
break continue return	<p>Do not use these statements within loops. Use of these statements in a loop causes Simulink HDL Coder to report the following error:</p> <p style="padding-left: 40px;">Unstructured flow graph or loop containing [statement type] not supported for HDL</p>
while	<p>while loops are not supported. Use of while loops causes Simulink HDL Coder to report the following error:</p> <p style="padding-left: 40px;">Unstructured flow graph or loop containing [statement type] not supported for HDL</p>
for	<p>for loops without static bounds are not supported. Use of for loops without static bounds causes Simulink HDL Coder to report the following error:</p> <p style="padding-left: 40px;">Unstructured flow graph or loop containing [statement type] not supported for HDL</p> <p>Do not use the &amp; and   operators within conditions of a for statement. Instead, use the &amp;&amp; and    operators.</p> <p>Embedded MATLAB does not support nonscalar expressions in the conditions of for statements. Use the all or any functions to collapse logical vectors into scalars.</p>

<b>Control Flow Statement</b>	<b>Notes</b>
if	<p>Do not use the &amp; and   operators within conditions of an if statement. Instead, use the &amp;&amp; and    operators.</p> <p>Embedded MATLAB does not support nonscalar expressions are not supported in the conditions of if statements. Use the all or any functions to collapse logical vectors into scalars.</p>
switch	<p>The HDL code matches the behavior of the MATLAB switch statement; the first matching case statement is executed.</p> <p>Use only scalars in conditional expressions in a switch statement.</p> <p>Use of fi variables in switch or case conditionals is not supported. For HDL code generation, the usage is restricted to uint8, uint16, uint32, sint8, sint16, and sint32.</p> <p>If multiple case statements make assignments to the same variable, then their numeric type and fimath specification should match that variable.</p>

## Other Limitations

This section lists other limitations that apply when generating HDL code with the Embedded MATLAB Function block. These limitations are:

- The HDL compatibility checker (checkhdl) performs only a basic compatibility check on the Embedded MATLAB Function block. HDL related warnings or errors may arise during code generation from an Embedded MATLAB Function block that is otherwise valid for simulation. Such errors are reported in a separate message window.
- Embedded MATLAB does not support nested functions. Subfunctions are supported, however. For an example, see “Tutorial Example: Incrementer” on page 10-6.
- Use of multiple values on the left side of an expression is not supported. For example, an error results from the following assignment statement:

```
[t1, t2, t3] = [1, 2, 3];
```

# Generating Scripts for HDL Simulators and Synthesis Tools

---

Overview of Script Generation for EDA Tools (p. 11-2)

Overview of generation of scripts for third-party simulation and synthesis tools

Defaults for Script Generation (p. 11-3)

Defaults and file naming conventions

Custom Script Generation (p. 11-4)

Command line properties and GUI options for customizing script files

### Overview of Script Generation for EDA Tools

Simulink HDL Coder supports generation of script files for third-party electronic design automation (EDA) tools. These scripts let you compile and simulate generated HDL code or synthesize generated HDL code.

Using the defaults, you can automatically generate scripts for the following tools:

- Mentor Graphics ModelSim SE/PE HDL simulator
- The Synplify family of synthesis tools

## Defaults for Script Generation

By default, script generation takes place automatically, as part of the code and test bench generation process.

All script files are generated in the target directory.

When you generate HDL code for a model or subsystem *system*, Simulink HDL Coder writes the following script files:

- *system\_compile.do*: ModelSim compilation script. This script contains commands to compile the generated code, but not to simulate it.
- *system\_synplify.tcl*: Synplify synthesis script

When you generate test bench code for a model or subsystem *system*, Simulink HDL Coder writes the following script files:

- *system\_tb\_compile.do*: ModelSim compilation script. This script contains commands to compile the generated code and test bench.
- *system\_tb\_sim.do*: ModelSim simulation script. This script contains commands to run a simulation of the generated code and test bench.

## Custom Script Generation

### In this section...

“Structure of Generated Script Files” on page 11-4

“Properties for Controlling Script Generation” on page 11-5

“Controlling Script Generation with the EDA Tool Scripts GUI Panel” on page 11-8

You can enable or disable script generation and customize the names and content of generated script files using either of the following methods:

- Use the `makehdl` or `makehdltb` functions, and pass in the appropriate property name/property value arguments, as described in “Properties for Controlling Script Generation” on page 11-5.
- Set script generation options in the **EDA Tool Scripts** pane of the Simulink HDL Coder GUI, as described in “Controlling Script Generation with the EDA Tool Scripts GUI Panel” on page 11-8.

### Structure of Generated Script Files

A generated EDA script consists of three sections, generated and executed in the following order:

- 1** An initialization (`Init`) phase. The `Init` phase performs any required setup actions, such as creating a design library or a project file. Some arguments to the `Init` phase are implicit, for example, the top-level entity or module name.
- 2** A command-per-file phase (`Cmd`). This phase of the script is called iteratively, once per generated HDL file or once per signal. On each call, a different file or signal name is passed in.
- 3** A termination phase (`Term`). This is the final execution phase of the script. One application of this phase is to execute a simulation of HDL code that was compiled in the `Cmd` phase. The `Term` phase takes no arguments.

Simulink HDL Coder generates scripts by passing format strings to the MATLAB `fprintf` function. Using the GUI options (or `makehdl` and



makehdltb properties) summarized in the following sections, you can pass in customized format strings to the script generator. Some of these format strings take arguments, such as the top-level entity or module name, or the names of the VHDL or Verilog files in the design.

You can use any legal `fprintf` formatting characters. For example, `'\n'` inserts a newline into the script file.

## Properties for Controlling Script Generation

This section describes how to set properties in the `makehdl` or `makehdltb` functions to enable or disable script generation and customize the names and content of generated script files.

### Enabling and Disabling Script Generation

The `EDAScriptGeneration` property controls the generation of script files. By default, `EDAScriptGeneration` is set `'on'`. To disable script generation, set `EDAScriptGeneration` to `'off'`, as in the following example.

```
makehdl('sfir_fixed/symmetric_fir','EDAScriptGeneration','off')
```

### Customizing Script Names

When you generate HDL code, script names are generated by appending a postfix string to the model or subsystem name *system*.

When you generate test bench code, script names are generated by appending a postfix string to the test bench name *testbench\_tb*.

The postfix string depends on the type of script (compilation, simulation, or synthesis) being generated. The default postfix strings are shown in the following table. For each type of script, you can define your own postfix using the associated property.

Script Type	Property	Default Value
Compilation	<code>'HDLCompileFilePostfix'</code>	<code>'_compile.do'</code>

Script Type	Property	Default Value
Simulation	'HDLSimFilePostfix'	'_sim.do'
Synthesis	'HDLSynthFilePostfix'	'_synplify.tcl'

The following command generates VHDL code for the subsystem `system`, specifying a custom postfix string for the compilation script. The name of the generated compilation script will be `system_test_compilation.do`.

```
makehdl('mymodel/system', 'HDLCompileFilePostfix', '_test_compilation.do')
```

### Customizing Script Code

Using the property name/property value pairs summarized in the following table, you can pass in customized format strings to `makehdl` or `makehdltb`. The properties are named according to the following conventions:

- Properties that apply to the initialization (`Init`) phase are identified by the substring `Init` in the property name.
- Properties that apply to the command-per-file phase (`Cmd`) are identified by the substring `Cmd` in the property name.
- Properties that apply to the termination (`Term`) phase are identified by the substring `Term` in the property name.

Property Name and Default	Description
Name: 'HDLCompileInit' Default: 'vlib work\n'	Format string passed to <code>fprintf</code> to write the <code>Init</code> section of the compilation script.
Name: 'HDLCompileVHDLCmd' Default: 'vcom %s %s\n'	Format string passed to <code>fprintf</code> to write the <code>Cmd</code> section of the compilation script for VHDL files. The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).

Property Name and Default	Description
Name: 'HDLCompileVerilogCmd' Default: 'vlog %s %s\n'	Format string passed to fprintf to write the Cmd section of the compilation script for Verilog files. The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: 'HDLCompileTerm' Default: ''	Format string passed to fprintf to write the termination portion of the compilation script.
Name: 'HDLSimInit' Default: ['onbreak resume\n',... 'onerror resume\n']	Format string passed to fprintf to write the initialization section of the simulation script.
Name: 'HDLSimCmd' Default: 'vsim work.%s\n'	Format string passed to fprintf to write the simulation command. The implicit argument is the top-level module or entity name.
Name: 'HDLSimViewWaveCmd' Default: 'add wave sim:%s\n'	Format string passed to fprintf to write the simulation script waveform viewing command. The implicit argument is the top-level module or entity name.
Name: 'HDLSimTerm' Default: 'run -all\n'	Format string passed to fprintf to write the Term portion of the simulation script
Name: 'HDLSynthInit' Default: 'project -new %s.prj\n'	Format string passed to fprintf to write the Init section of the synthesis script. The default string is a synthesis project creation command. The implicit argument is the top-level module or entity name.

Property Name and Default	Description
Name: 'HDLSynthCmd' Default: 'add_file %s\n'	Format string passed to fprintf to write the Cmd section of the synthesis script. The argument is the file name of the entity or module.
Name: 'HDLSynthTerm' Default:  <pre> ['set_option -technology VIRTEX4\n',... 'set_option -part XC4VSX35\n',... 'set_option -synthesis_onoff_pragma 0\n',... 'set_option -frequency auto\n',... 'project -run synthesis\n'] </pre>	Format string passed to fprintf to write the Term section of the synthesis script.

## Example

The following example specifies a ModelSim command for the Init phase of a compilation script for VHDL code generated from the subsystem system.

```
makehdl(system, 'HDLCompileInit', 'vlib mydesignlib\n')
```

The following example lists the resultant script, system\_compile.do.

```
vlib mydesignlib
vcom system.vhd
```

## Controlling Script Generation with the EDA Tool Scripts GUI Panel

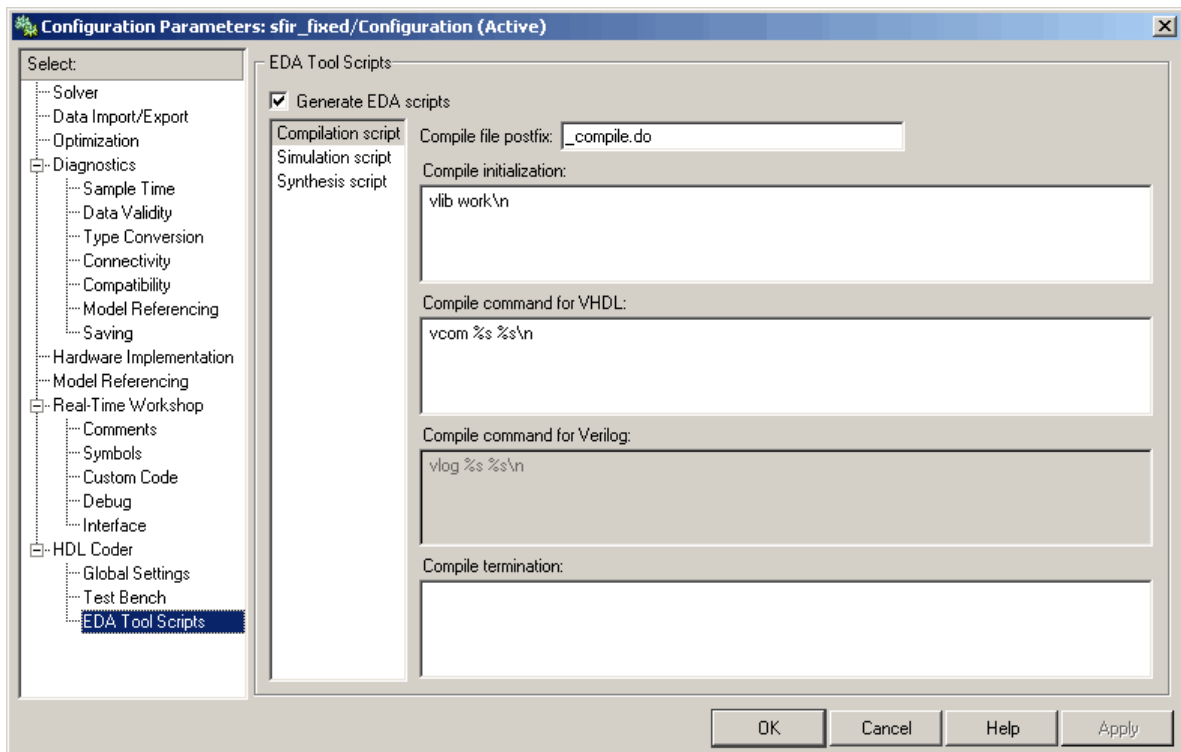
The **EDA Tool Scripts** panel of the Simulink HDL Coder GUI lets you set all options that control generation of script files. These options correspond to the properties described in “Properties for Controlling Script Generation” on page 11-5

To view and set options in the **EDA Tool Scripts** GUI panel:

- 1 Select **Configuration Parameters** from the **Simulation** menu in the model window.

The Configuration Parameters dialog box opens with the **Solver** options pane displayed.

- 2 Click the **EDA Tool Scripts** entry in the **Select** tree in the left panel of the Configuration Parameters dialog box. By default, the **EDA Tool Scripts** pane is displayed, with the **Compilation script** options group selected, as shown in the following figure.



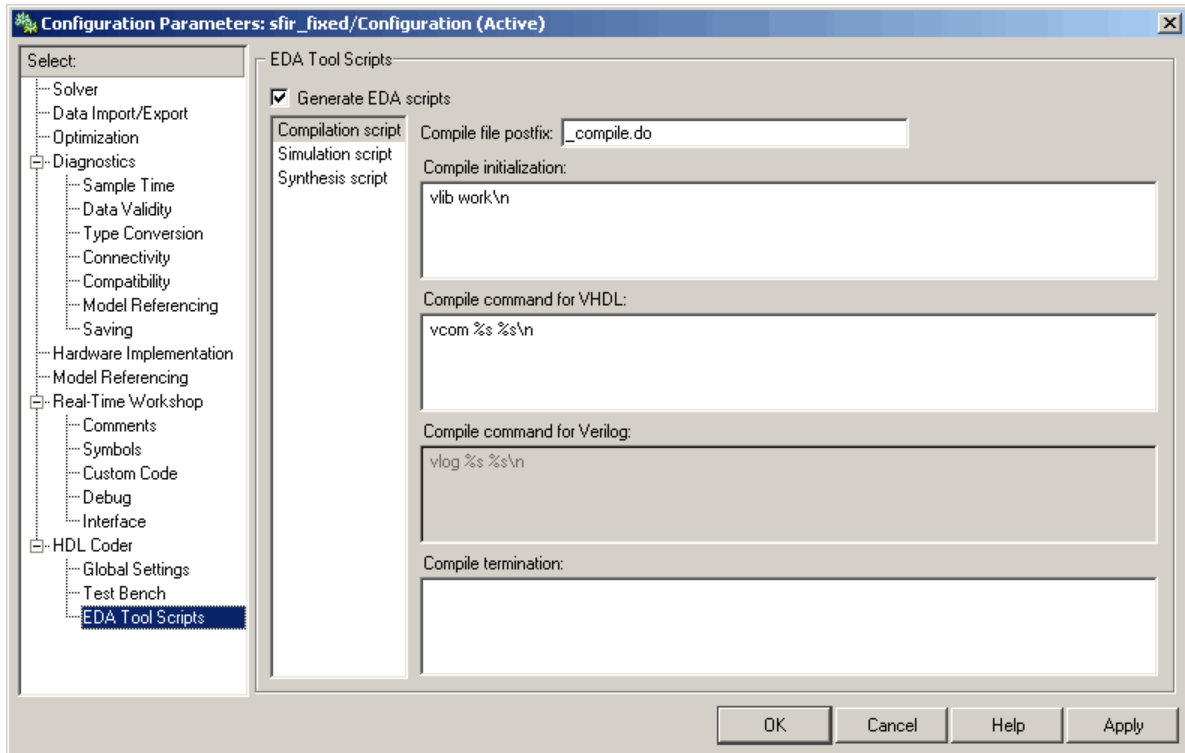
- 3 The **Generate EDA scripts** option controls the generation of script files. By default, this option is selected.

If you want to disable script generation, deselect this option and click **Apply**.

- 4** The list on the left of the **EDA Tool Scripts** pane lets you select from several categories of options. Select a category and set the options as desired. The categories are
- **Compilation script:** Options related to customizing scripts for compilation of generated VHDL or Verilog code. See “Compilation Script Options” on page 11-10 for further information.
  - **Simulation script:** Options related to customizing scripts for HDL simulators. See “Simulation Script Options” on page 11-12 for further information.
  - **Synthesis script:** Options related to customizing scripts for synthesis tools. See “Synthesis Script Options” on page 11-14 for further information.

### **Compilation Script Options**

The following figure shows the **Compilation script** pane, with all options set to their default values.



The following table summarizes the **Compilation script** options.

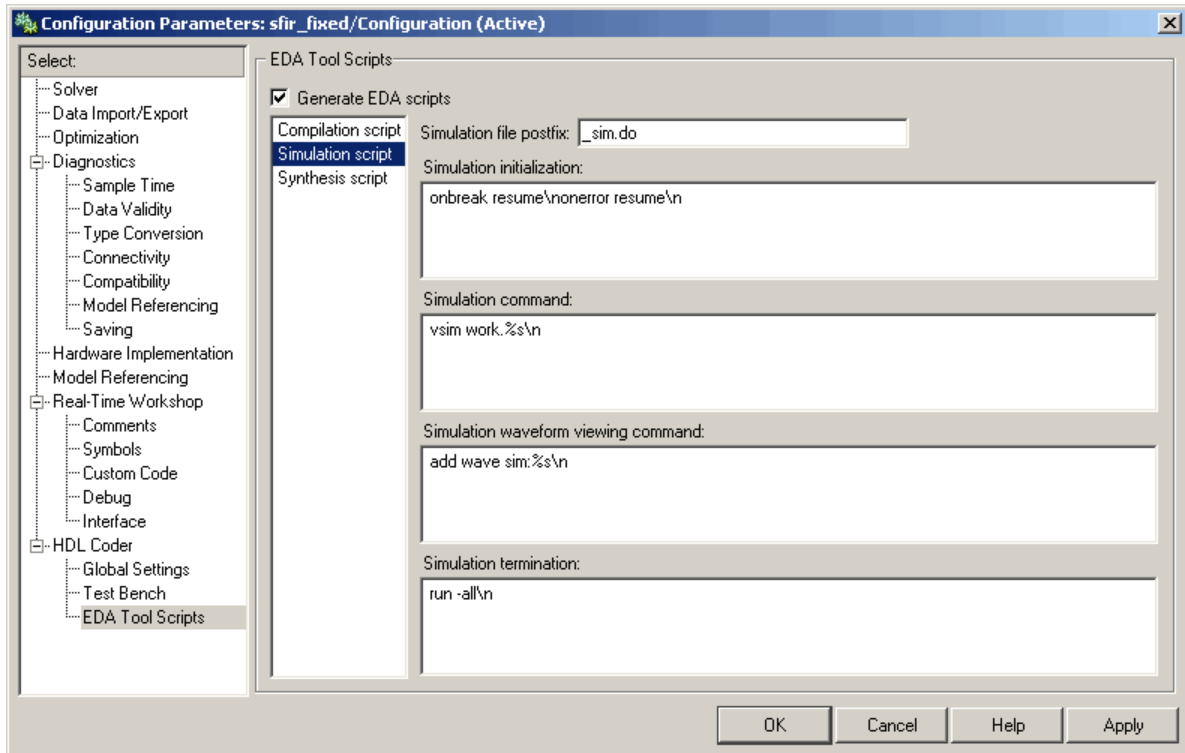
Option and Default	Description
<b>Compile file postfix'</b> '_compile.do'	Postfix string appended to the DUT name or test bench name to form the script file name.
Name: <b>Compile initialization</b> Default: 'vlib work\n'	Format string passed to fprintf to write the Init section of the compilation script.

Option and Default	Description
Name: <b>Compile command for VHDL</b> Default: 'vcom %s %s\n'	Format string passed to fprintf to write the Cmd section of the compilation script for VHDL files. The two arguments are the contents of the 'SimulatorFlags' property option and the filename of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: <b>Compile command for Verilog</b> Default: 'vlog %s %s\n'	Format string passed to fprintf to write the Cmd section of the compilation script for Verilog files. The two arguments are the contents of the 'SimulatorFlags' property and the filename of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: <b>Compile termination</b> Default: ''	Format string passed to fprintf to write the termination portion of the compilation script.

### Simulation Script Options

The following figure shows the **Simulation script** pane, with all options set to their default values.





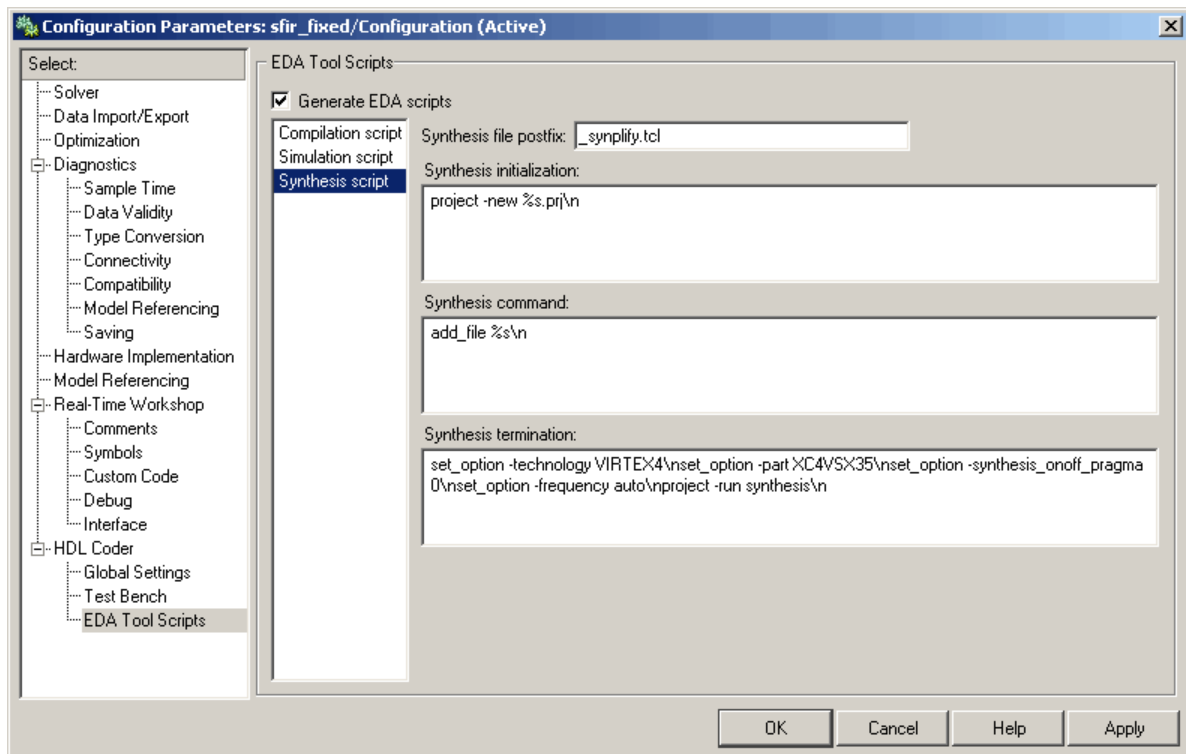
The following table summarizes the **Simulation script** options.

Option and Default	Description
<b>Simulation file postfix</b> Default: '_sim.do'	Postfix string appended to the model name or test bench name to form the simulation script file name.
<b>Simulation initialization</b> Default: ['onbreak resume\nnonerror resume\n']	Format string passed to fprintf to write the initialization section of the simulation script.
<b>Simulation command</b> Default: 'vsim work.%s\n'	Format string passed to fprintf to write the simulation command. The implicit argument is the top-level module or entity name.

Option and Default	Description
<b>Simulation waveform viewing command</b> Default: 'add wave sim:%s\n'	Format string passed to fprintf to write the simulation script waveform viewing command. The top-level module or entity signal names are implicit arguments.
<b>Simulation termination</b> Default: 'run -a11\n'	Format string passed to fprintf to write the Term portion of the simulation script.

## Synthesis Script Options

The following figure shows the **Synthesis script** pane, with all options set to their default values.



The following table summarizes the **Synthesis script** options.

Option Name and Default	Description
Name: <b>Synthesis initialization</b> Default: 'project -new %s.prj\n'	Format string passed to fprintf to write the Init section of the synthesis script. The default string is a synthesis project creation command. The implicit argument is the top-level module or entity name.
Name: <b>Synthesis command</b> Default: 'add_file %s\n'	Format string passed to fprintf to write the Cmd section of the synthesis script. The argument is the filename of the entity or module.
Name: <b>Synthesis termination</b> Default:  <pre> ['set_option -technology VIRTEX4\n',... 'set_option -part XC4VSX35\n',... 'set_option -synthesis_onoff_pragma 0\n',... 'set_option -frequency auto\n',... 'project -run synthesis\n'] </pre>	Format string passed to fprintf to write the Term section of the synthesis script.



# Properties — By Category

---

Language Selection Properties (p. 12-2)	Properties for selecting language of generated HDL code
File Naming and Location Properties (p. 12-2)	Properties that name and specify location of generated files
Reset Properties (p. 12-2)	Properties that specify reset signals in generated code
Header Comment and General Naming Properties (p. 12-3)	Properties affecting generation of header comments and process, module, component instance, and other name strings
Script Generation Properties (p. 12-4)	Properties affecting generation of script files for simulation and synthesis tools
Port Properties (p. 12-5)	Properties that specify port characteristics in generated code
Advanced Coding Properties (p. 12-6)	Advanced HDL coding properties
Test Bench Properties (p. 12-7)	Properties that specify generated test bench code
Generated Model Properties (p. 12-8)	Properties for controlling naming and appearance of generated models

## Language Selection Properties

TargetLanguage	Specify HDL language to use for generated code
----------------	--

## File Naming and Location Properties

HDLMapPostfix	Specify postfix string appended to file name for generated mapping file
TargetDirectory	Identify directory into which generated output files are written
VerilogFileExtension	Specify file type extension for generated Verilog files
VHDLFileExtension	Specify file type extension for generated VHDL files

## Reset Properties

ResetAssertedLevel	Specify asserted (active) level of reset input signal
ResetType	Specify whether to use asynchronous or synchronous reset logic when generating HDL code for registers
ResetValue	Specify constant value to which test bench forces reset input signals

## Header Comment and General Naming Properties

<code>ClockProcessPostfix</code>	Specify string to append to HDL clock process names
<code>EntityConflictPostfix</code>	Specify string to append to duplicate VHDL entity or Verilog module names
<code>InstancePrefix</code>	Specify string prefixed to generated component instance names
<code>PackagePostfix</code>	Specify string to append to specified model or subsystem name to form name of VHDL package file
<code>ReservedWordPostfix</code>	Specify string appended to identifiers for entities, signals, constants, or other model elements that conflict with VHDL or Verilog reserved words
<code>SplitArchFilePostfix</code>	Specify string to append to specified name to form name of file containing model's VHDL architecture
<code>SplitEntityArch</code>	Specify whether generated VHDL entity and architecture code is written to single VHDL file or to separate files
<code>SplitEntityFilePostfix</code>	Specify string to append to specified model name to form name of generated VHDL entity file
<code>VectorPrefix</code>	Specify string prefixed to vector names in generated code

## Script Generation Properties

EDAScriptGeneration	Enable or disable generation of script files for third-party tools
HDLCompileFilePostfix	Specify postfix string appended to file name for generated ModelSim compilation scripts
HDLCompileInit	Specify string written to initialization section of compilation script
HDLCompileTerm	Specify string written to termination section of compilation script
HDLCompileVerilogCmd	Specify command string written to compilation script for Verilog files
HDLCompileVHDLCmd	Specify command string written to compilation script for VHDL files
HDLSimCmd	Specify simulation command written to simulation script
HDLSimFilePostfix	Specify postfix string appended to file name for generated ModelSim test bench simulation scripts
HDLSimInit	Specify string written to initialization section of simulation script
HDLSimTerm	Specify string written to termination section of simulation script
HDLSimViewWaveCmd	Specify waveform viewing command written to simulation script
HDLSynthCmd	Specify command written to synthesis script
HDLSynthFilePostfix	Specify postfix string appended to file name for generated Synplify synthesis scripts



---

HDLSynthInit	Specify string written to initialization section of synthesis script
HDLSynthTerm	Specify string written to termination section of synthesis script

## Port Properties

ClockEnableInputPort	Name HDL port for model's clock enable input signals
ClockEnableOutputPort	Specify name of clock enable output port
ClockInputPort	Name HDL port for model's clock input signals
EnablePrefix	Specify base name string for internal clock enables in generated code
InputType	Specify HDL data type for model's input ports
OutputType	Specify HDL data type for model's output ports
ResetInputPort	Name HDL port for model's reset input

## Advanced Coding Properties

BlockGenerateLabel	Specify string to append to block labels used for HDL GENERATE statements
CastBeforeSum	Enable or disable type casting of input values for addition and subtraction operations before execution of operation
CheckHDL	Check model or subsystem for HDL code generation compatibility
ClockEnableDelay	Specify delay time applied to clock enable signals when reset is asserted
HDLControlFiles	Attach code generation control file to Simulink model
HoldInputDataBetweenSamples	Specify how long subrate signal values are held in valid state
InlineConfigurations	Specify whether generated VHDL code includes inline configurations
InstanceGenerateLabel	Specify string to append to instance section labels in VHDL GENERATE statements
LoopUnrolling	Specify whether VHDL FOR and GENERATE loops are unrolled and omitted from generated VHDL code
OutputGenerateLabel	Specify string that labels output assignment block for VHDL GENERATE statements
SafeZeroConcat	Specify syntax for concatenated zeros in generated VHDL code
UseAggregatesForConst	Specify whether all constants are represented by aggregates, including constants that are less than 32 bits

UserComment	Specify comment line in header of generated HDL and test bench files
UseRisingEdge	Specify VHDL coding style used to check for rising edges when operating on registers
UseVerilogTimescale	Use compiler `timescale directives in generated Verilog code
Verbosity	Specify level of detail for messages displayed during code generation

## Test Bench Properties

ClockHighTime	Specify period, in nanoseconds, during which test bench drives clock input signals high (1)
ClockLowTime	Specify period, in nanoseconds, during which test bench drives clock input signals low (0)
ForceClock	Specify whether test bench forces clock input signals
ForceClockEnable	Specify whether test bench forces clock enable input signals
ForceReset	Specify whether test bench forces reset input signals
HoldTime	Specify hold time for input signals and forced reset input signals
SimulatorFlags	Specify simulator flags to apply to generated compilation scripts

TestBenchPostFix	Specify suffix to test bench name
TestBenchReferencePostFix	Specify string appended to names of reference signals generated in test bench code

### Generated Model Properties

CodeGenerationOutput	Control production of generated code and display of generated model
GeneratedmodelName	Specify name of generated model
Generatedmodelnameprefix	Specify prefix to name of generated model
Highlightancestors	Highlight ancestors of blocks in generated model that differ from original model
Highlightcolor	Specify color for highlighted blocks in generated model

# Properties — Alphabetical List

---

# BlockGenerateLabel

---

<b>Purpose</b>	Specify string to append to block labels used for HDL GENERATE statements
<b>Settings</b>	'string' Specify a postfix string to append to block labels used for HDL GENERATE statements. The default string is <code>_gen</code> .
<b>See Also</b>	InstanceGenerateLabel, OutputGenerateLabel

<b>Purpose</b>	Enable or disable type casting of input values for addition and subtraction operations before execution of operation
<b>Settings</b>	'on' (default) Typecast input values in addition and subtraction operations to the result type before operating on the values. 'off' Preserve the types of input values during addition and subtraction operations and then convert the result to the result type.
<b>See Also</b>	InlineConfigurations, LoopUnrolling, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge, UseVerilogTimescale

# CheckHDL

---

<b>Purpose</b>	Check model or subsystem for HDL code generation compatibility
<b>Settings</b>	<p>'on'</p> <p>Check the model or subsystem for HDL compatibility before generating code, and report any problems encountered. This is equivalent to executing the checkhdl function before calling makehdl.</p> <p>'off' (default)</p> <p>Do not check the model or subsystem for HDL compatibility before generating code.</p>
<b>See Also</b>	checkhdl, makehdl



**Purpose** Specify delay time applied to clock enable signals when reset is asserted

**Settings** The `ClockEnableDelay` property specifies a delay time  $D$  ( number of base-rate clock cycles) applied to `clk_enable` signals when the model's reset input signal is asserted. `ClockEnableDelay` delay works in conjunction with the `HoldTime` property as follows:

- Where  $D = 0$ : After assertion of reset, `clk_enable` goes high after a delay equal to the specified by `HoldTime`.
- Where  $D \geq 1$ : After assertion of reset, `clk_enable` goes high after a delay of  $D$  base-rate clock cycles plus the delay specified by `HoldTime`.

The default value for  $D$  is 1.

**See Also** `HoldTime`

# ClockEnableInputPort

---

## Purpose

Name HDL port for model's clock enable input signals

## Settings

'string'

The default name for the model's clock enable input port is `clk_enable`.

If you override the default with (for example) the string `'filter_clock_enable'` for the generating subsystem `filter_subsys`, the generated entity declaration might look as follows:

```
ENTITY filter_subsys IS
    PORT( clk           : IN  std_logic;
          filter_clock_enable : IN  std_logic;
          reset         : IN  std_logic;
          filter_subsys_in  : IN  std_logic_vector (15 DOWNTO 0);
          filter_subsys_out : OUT std_logic_vector (15 DOWNTO 0);
    );
END filter_subsys;
```

If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`. See `ReservedWordPostfix` for more information.

## Usage Notes

The clock enable signal is asserted active high (1). Thus, the input value must be high for the generated entity's registers to be updated.

## See Also

`ClockInputPort`, `InputType`, `OutputType`, `ResetInputPort`

**Purpose** Specify name of clock enable output port

**Settings** 'string'

The default name for the generated clock enable output port is `ce_out`.

A clock enable output is generated when the design requires one.

# ClockHighTime

---

<b>Purpose</b>	Specify period, in nanoseconds, during which test bench drives clock input signals high (1)
<b>Settings</b>	ns The default is 5. The <code>ClockHighTime</code> and <code>ClockLowTime</code> properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.
<b>Usage Notes</b>	Simulink HDL Coder ignores this property if <code>ForceClock</code> is set to 'off'.
<b>See Also</b>	<code>ClockLowTime</code> , <code>ForceClock</code> , <code>ForceClockEnable</code> , <code>ForceReset</code> , <code>HoldTime</code>

**Purpose** Name HDL port for model's clock input signals

**Settings** 'string'

The default clock input port name is `clk`.

If you override the default with (for example) the string `'filter_clock'` for the generated entity `my_filter`, the generated entity declaration might look as follows:

```
ENTITY my_filter IS
  PORT( filter_clock : IN  std_logic;
        clk_enable   : IN  std_logic;
        reset        : IN  std_logic;
        my_filter_in  : IN  std_logic_vector (15 DOWNTO 0); -- sfix16_En15
        my_filter_out : OUT std_logic_vector (15 DOWNTO 0); -- sfix16_En15
  );
END my_filter;
```

If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`. See `ReservedWordPostfix` for more information.

**See Also** `ClockEnableInputPort`, `InputType`, `OutputType`

# ClockLowTime

---

<b>Purpose</b>	Specify period, in nanoseconds, during which test bench drives clock input signals low (0)
<b>Settings</b>	<p>The default is 5 ns.</p> <p>The <code>ClockHighTime</code> and <code>ClockLowTime</code> properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.</p>
<b>Usage Notes</b>	Simulink HDL Coder ignores this property if <code>ForceClock</code> is set to 'off'.
<b>See Also</b>	<code>ClockHighTime</code> , <code>ForceClock</code> , <code>ForceClockEnable</code> , <code>ForceReset</code> , <code>HoldTime</code>

**Purpose** Specify string to append to HDL clock process names

**Settings** 'string'

The default postfix is `_process`.

Simulink HDL Coder uses process blocks for register operations. The label for each of these blocks is derived from a register name and the postfix `_process`. For example, the coder derives the label `delay_pipeline_process` in the following block declaration from the register name `delay_pipeline` and the default postfix string `_process`:

```
delay_pipeline_process : PROCESS (clk, reset)
BEGIN
    .
    .
    .
```

**See Also** `PackagePostfix`, `ReservedWordPostfix`

# CodeGenerationOutput

---

**Purpose** Control production of generated code and display of generated model

**Settings**

- 'string'
- 'GenerateHDLCode' (default)  
Generate code but do not display the generated model.
- 'GenerateHDLCodeAndDisplayGeneratedModel'  
Generate both code and model, and display model when completed.
- 'DisplayGeneratedModelOnly'  
Create and display generated model, but do not proceed to code generation.

**See Also** “Defaults and Options for Generated Models” on page 6-12



<b>Purpose</b>	Enable or disable generation of script files for third-party tools
<b>Settings</b>	'on' (default) Enable generation of script files. 'off' Disable generation of script files.
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

# EnablePrefix

---

**Purpose** Specify base name string for internal clock enables in generated code

**Settings** 'string'

Specify the string used as the base name for internal clock enables and other flow control signals in generated code. The default string is 'enb'.

**Usage Notes** Where only a single clock enable is generated, EnablePrefix specifies the signal name for the internal clock enable signal.

In some cases multiple clock enables are generated (for example, when a cascade block implementation for certain blocks is specified). In such cases, EnablePrefix specifies a base signal name for the first clock enable that is generated. For other clock enable signals, numeric tags are appended to EnablePrefix to form unique signal names. For example, the following code fragment illustrates two clock enables that were generated when EnablePrefix was set to 'test\_clk\_enable' :

```
COMPONENT Timing_Controller
  PORT( clk           : IN    std_logic;
        reset        : IN    std_logic;
        clk_enable    : IN    std_logic;
        test_clk_enable : OUT  std_logic;
        test_clk_enable_5_1_0 : OUT  std_logic
  );
END COMPONENT;
```

<b>Purpose</b>	Specify string to append to duplicate VHDL entity or Verilog module names
<b>Settings</b>	'string'  The specified postfix resolves duplicate VHDL entity or Verilog module names. The default string is <code>_entity</code> .  For example, if Simulink HDL Coder detects two entities with the name <code>MyFilt</code> , the coder names the first entity <code>MyFilt</code> and the second instance <code>MyFilt_entity</code> .
<b>See Also</b>	<code>PackagePostfix</code> , <code>ReservedWordPostfix</code>

# ForceClock

---

## **Purpose**

Specify whether test bench forces clock input signals

## **Settings**

'on' (default)

Specify that the test bench forces the clock input signals. When this option is set, the clock high and low time settings control the clock waveform.

'off'

Specify that a user-defined external source forces the clock input signals.

## **See Also**

ClockLowTime, ClockHighTime, ForceClockEnable, ForceReset, HoldTime

<b>Purpose</b>	Specify whether test bench forces clock enable input signals
<b>Settings</b>	<p>'on' (default)</p> <p>Specify that the test bench forces the clock enable input signals to active high (1) or active low (0), depending on the setting of the clock enable input value.</p> <p>'off'</p> <p>Specify that a user-defined external source forces the clock enable input signals.</p>
<b>See Also</b>	ClockHighTime, ClockLowTime, ForceClock, HoldTime

# ForceReset

---

## **Purpose**

Specify whether test bench forces reset input signals

## **Settings**

'on' (default)

Specify that the test bench forces the reset input signals. If you enable this option, you can also specify a hold time to control the timing of a reset.

'off'

Specify that a user-defined external source forces the reset input signals.

## **See Also**

ClockHighTime, ClockLowTime, ForceClock, HoldTime

**Purpose** Specify name of generated model

**Settings** 'string'

By default, the name of a generated model is the same as that of the original model. Assign a string value to GeneratedmodelName to override the default.

**See Also** “Defaults and Options for Generated Models” on page 6-12

# GeneratedmodelNameprefix

---

<b>Purpose</b>	Specify prefix to name of generated model
<b>Settings</b>	'string' The default prefix is 'gm_'.
<b>See Also</b>	“Defaults and Options for Generated Models” on page 6-12



<b>Purpose</b>	Specify string written to initialization section of compilation script
<b>Settings</b>	'string' The default string is 'vlib work\n'.
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

# HDLCompileTerm

---

<b>Purpose</b>	Specify string written to termination section of compilation script
<b>Settings</b>	'string' The default is the null string ('').
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

**Purpose** Specify postfix string appended to file name for generated ModelSim compilation scripts

**Settings** 'string'

The default postfix is `_compile.do`.

For example, if the name of the device under test or test bench is `my_design`, Simulink HDL Coder adds the postfix `_compile.do` to form the name `my_design_compile.do`.

# HDLCompileVerilogCmd

---

**Purpose** Specify command string written to compilation script for Verilog files

**Settings** 'string'

The default string is 'vlog %s %s\n'.

The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).

**See Also** Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

**Purpose** Specify command string written to compilation script for VHDL files

**Settings** 'string'

The default string is 'vcom %s %s\n'.

The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).

**See Also** Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

# HDLControlFiles

---

## Purpose

Attach code generation control file to Simulink model

## Settings

{'string'}

Pass in a cell array containing a string that specifies a control file to be attached to the current model. Defaults are

- File name extension: `.m`
- Path: the control file must be on the MATLAB path or in the current working directory. You can enter either a full path name or a relative path.

---

**Note** The current release supports specification of a single control file.

---

## Usage Notes

To clear the property (so that no control file is invoked during code generation), pass in a cell array containing the null string, as in the following example:

```
makehdl(gcb, 'HDLControlFiles', {' '});
```

## See Also

For a detailed description of the structure and use of control files, see Chapter 5, “Code Generation Control Files”.

**Purpose** Specify postfix string appended to file name for generated mapping file

**Settings** 'string'

The default postfix is '\_map.txt'.

For example, if the name of the device under test is my\_design, Simulink HDL Coder adds the postfix \_map.txt to form the name my\_design\_map.txt.

# HDLsimCmd

---

**Purpose** Specify simulation command written to simulation script

**Settings** 'string'

The default string is 'vsim work.%s\n'.

The implicit argument is the top-level module or entity name.

**See Also** Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”



<b>Purpose</b>	Specify string written to initialization section of simulation script
<b>Settings</b>	'string' The default string is <pre>['onbreak resume\n',... 'onerror resume\n']</pre>
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

# HDLSimFilePostfix

---

**Purpose** Specify postfix string appended to file name for generated ModelSim test bench simulation scripts

**Settings** 'string'

The default postfix is `_sim.do`.

For example, if the name of your test bench file is `my_design`, Simulink HDL Coder adds the postfix `_sim.do` to form the name `my_design_tb_sim.do`.

<b>Purpose</b>	Specify string written to termination section of simulation script
<b>Settings</b>	'string' The default string is 'run -all\n'.
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

# HDLsimViewWaveCmd

---

**Purpose** Specify waveform viewing command written to simulation script

**Settings** 'string'

The default string is 'add wave sim:%s\n'

The implicit argument is the top-level module or entity name.

**See Also** Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

<b>Purpose</b>	Specify command written to synthesis script
<b>Settings</b>	'string' The default string is 'add_file %s\n'. The implicit argument is the file name of the entity or module.
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

# HDLSynthInit

---

<b>Purpose</b>	Specify string written to initialization section of synthesis script
<b>Settings</b>	'string' The default string is 'project -new %s.prj\n', which is a synthesis project creation command. The implicit argument is the top-level module or entity name.
<b>See Also</b>	Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”

**Purpose**

Specify postfix string appended to file name for generated Synplify synthesis scripts

**Settings**

'string'

The default postfix is `_synplify.tcl`.

For example, if the name of the device under test is `my_design`, Simulink HDL Coder adds the postfix `_synplify.tcl` to form the name `my_design_synplify.tcl`.

**Purpose** Specify string written to termination section of synthesis script

**Settings** 'string'

The default string is

```
['set_option -technology VIRTEX4\n',...  
'set_option -part XC4VSX35\n',...  
'set_option -synthesis_onoff_pragma 0\n',...  
'set_option -frequency auto\n',...  
'project -run synthesis\n']
```

**See Also** Chapter 11, “Generating Scripts for HDL Simulators and Synthesis Tools”



<b>Purpose</b>	Highlight ancestors of blocks in generated model that differ from original model
<b>Settings</b>	'on' (default) Highlight blocks in a generated model that differ from the original model, and their ancestor (parent) blocks in the model hierarchy. 'off' Highlight only the blocks in a generated model that differ from the original model without highlighting their ancestor (parent) blocks in the model hierarchy.
<b>See Also</b>	“Defaults and Options for Generated Models” on page 6-12

# Highlightcolor

---

**Purpose** Specify color for highlighted blocks in generated model

**Settings** 'string'

The default color specification is 'cyan'.

Specify the color as one of the following color string values:

- cyan
- yellow
- magenta
- red
- green
- blue
- white
- black

**See Also** “Defaults and Options for Generated Models” on page 6-12

# HoldInputDataBetweenSamples

---

## **Purpose**

Specify how long subrate signal values are held in valid state

## **Settings**

This property determines how long (in terms of base-rate clock cycles) data values for subrate signals are held in a valid state.

For subrate signals, N base-rate clock cycles elapse per subrate sample period (where  $N \geq 2$ ). When `HoldInputDataBetweenSamples` is set 'on' (the default), data values for subrate signals are held in a valid state across N base-rate clock cycles.

When `HoldInputDataBetweenSamples` is set 'off', data values for subrate signals are held in a valid state for only one base-rate clock cycle. For the subsequent base-rate cycles, data is in an unknown state (expressed as 'X') until leading edge of the next subrate sample period.

## **See Also**

`HoldTime`

# HoldTime

## Purpose

Specify hold time for input signals and forced reset input signals

## Settings

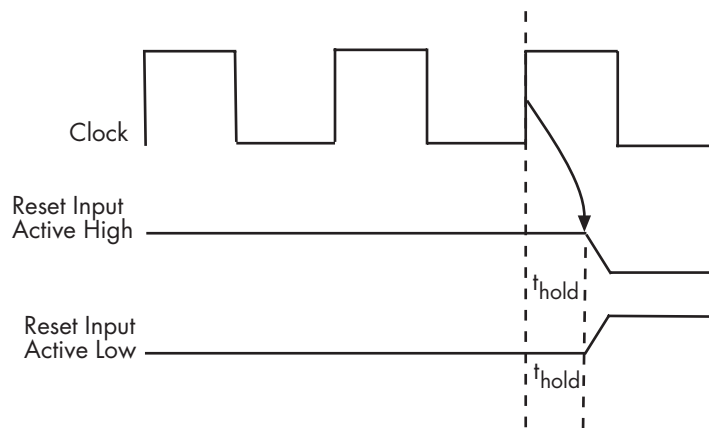
ns

Specify the number of nanoseconds (a positive integer) during which the model's data input signals and forced reset input signals are held past the clock rising edge. The default is 2.

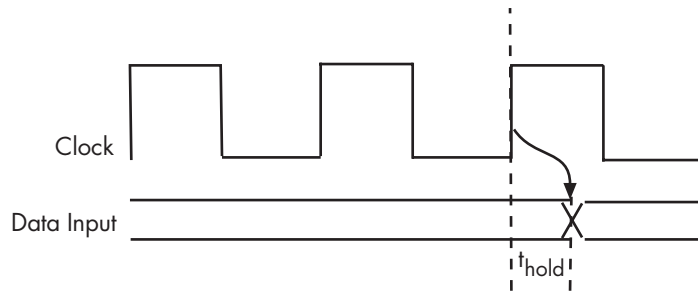
This option applies to reset input signals only if forced resets are enabled.

## Usage Notes

The hold time is the amount of time that reset input signals and input data are held past the clock rising edge. The following figures show the application of a hold time ( $t_{\text{hold}}$ ) for reset and data input signals when the signals are forced to active high and active low.



**Hold Time for Reset Input Signals**



## Hold Time for Data Input Signals

---

**Note** A reset signal is always asserted for two cycles plus  $t_{hold}$ .

---

## See Also

ClockHighTime, ClockLowTime, ForceClock

# InlineConfigurations

---

<b>Purpose</b>	Specify whether generated VHDL code includes inline configurations
<b>Settings</b>	'on' (default) Include VHDL configurations in any file that instantiates a component. 'off' Suppress the generation of configurations and require user-supplied external configurations. Use this setting if you are creating your own VHDL configuration files.
<b>Usage Notes</b>	VHDL configurations can be either inline with the rest of the VHDL code for an entity or external in separate VHDL source files. By default, Simulink HDL Coder includes configurations for a model within the generated VHDL code. If you are creating your own VHDL configuration files, you should suppress the generation of inline configurations.
<b>See Also</b>	LoopUnrolling, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge

<b>Purpose</b>	Specify HDL data type for model's input ports
<b>Settings</b>	<p>'std_logic_vector'</p> <p>Specifies VHDL type STD_LOGIC_VECTOR for the model's input ports.</p> <p>'signed/unsigned'</p> <p>Specifies VHDL type SIGNED or UNSIGNED for the model's input ports.</p> <p>'wire' (Verilog)</p> <p>If the target language is Verilog, the data type for all ports is wire. This property is not modifiable in this case.</p>
<b>See Also</b>	ClockEnableInputPort, , OutputType

# InstanceGenerateLabel

---

<b>Purpose</b>	Specify string to append to instance section labels in VHDL GENERATE statements
<b>Settings</b>	'string' Specify a postfix string to append to instance section labels in VHDL GENERATE statements. The default string is <code>_gen</code> .
<b>See Also</b>	BlockGenerateLabel, OutputGenerateLabel



**Purpose** Specify string prefixed to generated component instance names

**Settings** 'string'  
Specify a string to be prefixed to component instance names in generated code. The default string is u\_.

# LoopUnrolling

---

<b>Purpose</b>	Specify whether VHDL FOR and GENERATE loops are unrolled and omitted from generated VHDL code
<b>Settings</b>	<p>'on'</p> <p>Unroll and omit FOR and GENERATE loops from the generated VHDL code.</p> <p>In Verilog code, loops are always unrolled.</p> <p>If you are using an electronic design automation (EDA) tool that does not support GENERATE loops, you can enable this option to omit loops from your generated VHDL code.</p> <p>'off' (default)</p> <p>Include FOR and GENERATE loops in the generated VHDL code.</p>
<b>Usage Notes</b>	The setting of this option does not affect results obtained from simulation or synthesis of generated VHDL code.
<b>See Also</b>	InlineConfigurations, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge

<b>Purpose</b>	Specify string that labels output assignment block for VHDL GENERATE statements
<b>Settings</b>	'string'  Specify a postfix string to append to output assignment block labels in VHDL GENERATE statements. The default string is outputgen.
<b>See Also</b>	BlockGenerateLabel, OutputGenerateLabel

# OutputType

---

<b>Purpose</b>	Specify HDL data type for model's output ports
<b>Settings</b>	'std_logic_vector' (VHDL default) Output ports have VHDL type STD_LOGIC_VECTOR. 'signed/unsigned' Output ports have type SIGNED or UNSIGNED. 'wire' (Verilog) If the target language is Verilog, the data type for all ports is wire. This property is not modifiable in this case.
<b>See Also</b>	ClockEnableInputPort, InputType

<b>Purpose</b>	Specify string to append to specified model or subsystem name to form name of VHDL package file
<b>Settings</b>	'string'  The coder applies this option only if a package file is required for the design. The default string is <code>_pkg</code> .
<b>See Also</b>	<code>ClockProcessPostfix</code> , <code>EntityConflictPostfix</code> , <code>ReservedWordPostfix</code>

# ReservedWordPostfix

---

**Purpose** Specify string appended to identifiers for entities, signals, constants, or other model elements that conflict with VHDL or Verilog reserved words

**Settings** 'string'  
The default postfix is `_rsvd`.  
The reserved word postfix is applied identifiers (for entities, signals, constants, or other model elements) that conflict with VHDL or Verilog reserved words. For example, if your generating model contains a signal named `mod`, Simulink HDL Coder adds the postfix `_rsvd` to form the name `mod_rsvd`.

**See Also** `ClockProcessPostfix`, `EntityConflictPostfix`, `ReservedWordPostfix`

**Purpose**

Specify asserted (active) level of reset input signal

**Settings**

'active-high' (default)

Specify that the reset input signal must be driven high (1) to reset registers in the model. For example, the following code fragment checks whether reset is active high before populating the delay\_pipeline register:

```
Delay_Pipeline_Process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        delay_pipeline(0 TO 50) <= (OTHERS => (OTHERS => '0'));
    .
    .
    .
```

'active-low'

Specify that the reset input signal must be driven low (0) to reset registers in the model. For example, the following code fragment checks whether reset is active low before populating the delay\_pipeline register:

```
Delay_Pipeline_Process : PROCESS (clk, reset)
BEGIN
    IF reset = '0' THEN
        delay_pipeline(0 TO 50) <= (OTHERS => (OTHERS => '0'));
    .
    .
    .
```

**See Also**

ResetType

# ResetInputPort

---

**Purpose** Name HDL port for model's reset input

**Settings** 'string'

The default name for the model's reset input port is `reset`.

If you override the default with (for example) the string `'chip_reset'` for the generating system `myfilter`, the generated entity declaration might look as follows:

```
ENTITY myfilter IS
    PORT( clk           : IN  std_logic;
          clk_enable    : IN  std_logic;
          chip_reset    : IN  std_logic;
          myfilter_in   : IN  std_logic_vector (15 DOWNT0 0);
          myfilter_out  : OUT std_logic_vector (15 DOWNT0 0);
    );
END myfilter;
```

If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`. See `ReservedWordPostfix` for more information.

**Usage Notes** If the reset asserted level is set to active high, the reset input signal is asserted active high (1) and the input value must be high (1) for the entity's registers to be reset. If the reset asserted level is set to active low, the reset input signal is asserted active low (0) and the input value must be low (0) for the entity's registers to be reset.

**See Also** `ClockEnableInputPort`, `InputType`, `OutputType`



## Purpose

Specify whether to use asynchronous or synchronous reset logic when generating HDL code for registers

## Settings

'async' (default)

Use asynchronous reset logic. The following process block, generated by a Unit Delay block, illustrates the use of asynchronous resets. When the reset signal is asserted, the process block performs a reset, without checking for a clock event.

```
Unit_Delay1_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay1_out1 <= (OTHERS => '0');
    ELSIF clk'event AND clk = '1' THEN
        IF clk_enable = '1' THEN
            Unit_Delay1_out1 <= signed(x_in);
        END IF;
    END IF;
END PROCESS Unit_Delay1_process;
```

'sync'

Use synchronous reset logic. Code for a synchronous reset follows. The following process block, generated by a Unit Delay block, checks for a clock event, the rising edge, before performing a reset:

```
Unit_Delay1_process : PROCESS (clk)
BEGIN
    IF rising_edge(clk) THEN
        IF reset = '1' THEN
            Unit_Delay1_out1 <= (OTHERS => '0');
        ELSIF clk_enable = '1' THEN
            Unit_Delay1_out1 <= signed(x_in);
        END IF;
    END IF;
```

# ResetType

---

```
END PROCESS Unit_Delay1_process;
```

## See Also

`ResetAssertedLevel`

<b>Purpose</b>	Specify constant value to which test bench forces reset input signals
<b>Settings</b>	'active high' (default) Specify that the test bench set the reset input signal to active high (1). 'active low' Specify that the test bench set the reset input signal to active low (0).
<b>Usage Notes</b>	The setting for this option must match the setting of the reset asserted level specified for the test bench. Simulink HDL Coder ignores the setting of this option if forced resets are disabled.
<b>See Also</b>	ForceReset, ResetType, ResetAssertedLevel

# SafeZeroConcat

---

<b>Purpose</b>	Specify syntax for concatenated zeros in generated VHDL code
<b>Settings</b>	'on' (default) Use the type-safe syntax, '0' & '0', for concatenated zeros. Typically, this syntax is preferred.  'off' Use the syntax "000000..." for concatenated zeros. This syntax can be easier to read and is more compact, but it can lead to ambiguous types.
<b>See Also</b>	LoopUnrolling, UseAggregatesForConst, UseRisingEdge

<b>Purpose</b>	Specify simulator flags to apply to generated compilation scripts
<b>Settings</b>	'string' Specify options that are specific to your application and the simulator you are using. For example, if you must use the 1076–1993 VHDL compiler, specify the flag -93.
<b>Usage Notes</b>	The flags you specify with this option are added to the compilation command in generated compilation scripts. The simulation command string is specified by the HDLCompileVHDLCmd or HDLCompileVerilogCmd properties.

# SplitArchFilePostfix

---

<b>Purpose</b>	Specify string to append to specified name to form name of file containing model's VHDL architecture
<b>Settings</b>	'string'  The default is <code>_arch</code> . This option applies only if you direct Simulink HDL Coder to place the generated VHDL entity and architecture code in separate files.
<b>Usage Notes</b>	The option applies only if you direct Simulink HDL Coder to place the filter's entity and architecture in separate files.
<b>See Also</b>	<code>SplitEntityArch</code> , <code>SplitEntityFilePostfix</code>

## Purpose

Specify whether generated VHDL entity and architecture code is written to single VHDL file or to separate files

## Settings

'on'

Write the generated VHDL code to a single file.

'off' (default)

Write the code for the generated VHDL entity and architecture to separate files.

The names of the entity and architecture files derive from the base file name (as specified by the generating model or subsystem name). By default, postfix strings identifying the file as an entity (`_entity`) or architecture (`_arch`) are appended to the base file name. You can override the default and specify your own postfix string.

For example, instead of all generated code residing in `MyFIR.vhd`, you can specify that the code reside in `MyFIR_entity.vhd` and `MyFIR_arch.vhd`.

---

**Note** This property is specific to VHDL code generation. It does not apply to Verilog code generation and should not be enabled when generating Verilog code.

---

## See Also

`SplitArchFilePostfix`, `SplitEntityFilePostfix`

# SplitEntityFilePostfix

---

**Purpose** Specify string to append to specified model name to form name of generated VHDL entity file

**Settings** 'string'  
The default is `_entity`. This option applies only if you direct Simulink HDL Coder to place the generated VHDL entity and architecture code in separate files.

**See Also** SplitArchFilePostfix, SplitEntityArch



**Purpose** Identify directory into which generated output files are written

**Settings** 'string'

Specify a subdirectory under the current working directory into which generated files are written. The string can specify a complete path name. The default string is hdlsrc.

If the target directory does not exist, Simulink HDL Coder creates it.

**See Also** VerilogFileExtension, VHDLFileExtension

# TargetLanguage

---

**Purpose** Specify HDL language to use for generated code

**Settings**

- 'VHDL' (default)  
Generate VHDL filter code.
- 'verilog'  
Generate Verilog filter code.

**Purpose** Specify suffix to test bench name

**Settings** 'string'

The default postfix is '\_tb'.

For example, if the name of your DUT is my\_test, Simulink HDL Coder adds the postfix \_tb to form the name my\_test\_tb.

# TestBenchReferencePostFix

---

**Purpose** Specify string appended to names of reference signals generated in test bench code

**Settings** 'string'  
The default postfix is '\_ref'.  
Reference signal data is represented as arrays in the generated test bench code. The string specified by TestBenchReferencePostFix is appended to the generated signal names.

## Purpose

Specify whether all constants are represented by aggregates, including constants that are less than 32 bits

## Settings

'on'

Specify that all constants, including constants that are less than 32 bits, be represented by aggregates. The following VHDL constant declarations show scalars less than 32 bits being declared as aggregates:

```
CONSTANT coeff1 :signed(15 DOWNT0 0) := (4 DOWNT0 2 => '0', 0 =>'0', OTHERS => ', ');
CONSTANT coeff2 :signed(15 DOWNT0 0) := (6 => '0', 4 DOWNT0 3 => '0',OTHERS => ', ');
```

'off' (default)

Specify that the coder represent constants less than 32 bits as scalars and constants greater than or equal to 32 bits as aggregates. The following VHDL constant declarations are examples of declarations generated by default for values less than 32 bits:

```
CONSTANT coeff1 :signed(15 DOWNT0 0) := to_signed(-30, 16); -- sfix16_En15
CONSTANT coeff2 :signed(15 DOWNT0 0) := to_signed(-89, 16); -- sfix16_En15
```

## See Also

LoopUnrolling, SafeZeroConcat, UseRisingEdge

# UserComment

---

**Purpose** Specify comment line in header of generated HDL and test bench files

**Settings** 'string'

The comment is generated in each of the generated code and test bench files. The code generator adds leading comment characters as appropriate for the target language. When newlines or line feeds are included in the string, the code generator emits single-line comments for each newline.

For example, the following makehdl command adds two comment lines to the header in a generated VHDL file.

```
makehdl(gcb, 'UserComment', 'This is a comment line.\nThis is a second line.')
```

The resulting header comment block for subsystem `symmetric_fir` would appear as follows:

```
-- -----  
--  
-- Module: symmetric_fir  
-- Simulink Path: sfir_fixed/symmetric_fir  
-- Created: 2006-11-20 15:55:25  
-- Hierarchy Level: 0  
--  
-- This is a comment line.  
-- This is a second line.  
--  
-- Simulink model description for sfir_fixed:  
-- This model shows how to use Simulink HDL Coder to check, generate,  
-- and verify HDL for a fixed-point symmetric FIR filter.  
--  
-- -----
```

## Purpose

Specify VHDL coding style used to check for rising edges when operating on registers

## Settings

'on'

Use the VHDL `rising_edge` function to check for rising edges when operating on registers. The following code, generated from a Unit Delay block, tests `rising_edge` as shown in the following PROCESS block:

```
Unit_Delay1_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay1_out1 <= (OTHERS => '0');
    ELSIF rising_edge(clk) THEN
        IF clk_enable = '1' THEN
            Unit_Delay1_out1 <= signed(x_in);
        END IF;
    END IF;
END PROCESS Unit_Delay1_process;
```

'off' (default)

Check for clock events when operating on registers. The following code, generated from a Unit Delay block, checks for a clock event as shown in the ELSIF statement of the following PROCESS block:

```
Unit_Delay1_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay1_out1 <= (OTHERS => '0');
    ELSIF clk'event AND clk = '1' THEN
        IF clk_enable = '1' THEN
            Unit_Delay1_out1 <= signed(x_in);
        END IF;
    END IF;
```

# UseRisingEdge

---

```
END PROCESS Unit_Delay1_process;
```

## **Usage Notes**

The two coding styles have different simulation behavior when the clock transitions from 'x' to '1'.

## **See Also**

LoopUnrolling, SafeZeroConcat, UseAggregatesForConst



<b>Purpose</b>	Use compiler <code>`timescale</code> directives in generated Verilog code
<b>Settings</b>	<code>'on'</code> (default) Use compiler <code>`timescale</code> directives in generated Verilog code. <code>'off'</code> Suppress the use of compiler <code>`timescale</code> directives in generated Verilog code.
<b>Usage Notes</b>	The <code>`timescale</code> directive provides a way of specifying different delay values for multiple modules in a Verilog file. This setting does not affect the generated test bench.
<b>See Also</b>	<code>LoopUnrolling</code> , <code>SafeZeroConcat</code> , <code>UseAggregatesForConst</code> , <code>UseRisingEdge</code>

# VectorPrefix

---

**Purpose** Specify string prefixed to vector names in generated code

**Settings** 'string'  
Specify a string to be prefixed to vector names in generated code. The default string is `vector_of_.`

**Purpose** Specify level of detail for messages displayed during code generation

**Settings**

n

The default for n is 0 (minimal messages displayed).

When `Verbosity` is set to 0, minimal code generation progress messages are displayed in the MATLAB window. When `Verbosity` is set to 1, more detailed progress messages are displayed.

# VerilogFileExtension

---

**Purpose** Specify file type extension for generated Verilog files

**Settings** 'string'  
The default file type extension for generated Verilog files is .v.

**See Also** TargetLanguage

<b>Purpose</b>	Specify file type extension for generated VHDL files
<b>Settings</b>	'string' The default file type extension for generated VHDL files is .vhd.
<b>See Also</b>	TargetLanguage

# VHDLFileExtension

---

# Functions — Alphabetical List

---

# checkhdl

---

**Purpose** Check subsystem or model for compatibility with HDL code generation

**Syntax**

```
checkhdl
checkhdl(bdroot)
checkhdl('modelName')
checkhdl('modelName/subsys')
checkhdl(gcf)
output = checkhdl(arg)
```

**Description** `checkhdl` is a utility that checks a subsystem or model for compatibility with HDL code generation. If any incompatibilities are detected (for example, use of unsupported blocks or illegal data type usage), `checkhdl` displays information on the blocks and potential problems in an HTML report.

`checkhdl` examines (by default) the current Simulink model for compatibility with HDL code generation.

`checkhdl(bdroot)` examines the current Simulink model for compatibility with HDL code generation.

`checkhdl('modelName')` examines the Simulink model explicitly specified by 'modelName' for compatibility with HDL code generation.

`checkhdl('modelName/subsys')` examines a specified subsystem within the Simulink model specified by 'modelName' for compatibility with HDL code generation.

'subsys' specifies the name of the subsystem to be checked. In the current release, 'subsys' must be at the top (root) level of the current Simulink model; it cannot be a subsystem nested at a lower level of the model hierarchy.

`checkhdl(gcf)` examines the currently selected subsystem within the current Simulink model for compatibility with HDL code generation.

`checkhdl` generates an HTML HDL Code Generation Check Report. The report file-naming convention is `system_report.html`, where `system` is the name of the subsystem or model that was passed in to



checkhdl. The report is written to the target directory. checkhdl also displays the report in a browser window.

The report is in table format. Each entry in the table is hyperlinked to a block or subsystem that caused a problem. When you click the hyperlink, Simulink highlights and displays the block of interest (provided that the model referenced by the report is open).

If no errors are encountered, the report contains only a hyperlink to the subsystem or model that was checked.

Alternatively, you can also specify an output argument, using the following syntax:

```
output = checkhdl(arg)
```

where *arg* specifies a model or subsystem in any of the forms described previously.

When an output argument is specified, checkhdl returns a 1×N MATLAB struct array with one entry for each error, warning or message. In this case, no report is generated (see “Examples” on page 14-4).

The MathWorks strongly recommends that you use checkhdl to check your subsystems or models before generating HDL code.

checkhdl reports three levels of compatibility problems:

- *Errors*: Errors will cause makehdl to error out. These issues must be fixed before HDL code can be generated. A typical error would be the use of an unsupported data type. For example, the current release does not support complex numbers.
- *Warnings*: Warnings may cause problems in the generated code, but generally allow HDL code generation to continue. For example, the presence of an unsupported block in the model would raise a warning. In this case, the code generator attempts to proceed as if the block were not present in the design. This could lead to errors later in the code generation process, which would then terminate.

- *Messages*: Messages are indications that the HDL code generator may treat data types in a way that differs from what might be expected. For example, single-precision floating-point data types are automatically converted to double-precision because neither VHDL nor Verilog support single-precision data types.

---

**Note** If a model or subsystem passes checkhdl without errors, that does *not* imply that makehdl will complete successfully, since not all block parameters are verified in this release. However, if checkhdl reports an error, makehdl will not successfully complete HDL code generation.

For convenience, checkhdl also takes the same property-value pairs as makehdl and makehdltb.

---

## Examples

The following example checks the subsystem `symmetric_fir` within the model `sfir_fixed` for HDL code generation compatibility. If problems are encountered, an HTML report is generated.

```
checkhdl('sfir_fixed/symmetric_fir')
```

The following example checks the subsystem `symmetric_fir_err` within the model `sfir_fixed_err` for HDL code generation compatibility. Information on problems encountered is returned in the struct output. The first element of output is then displayed.

```
output = checkhdl('sfir_fixed_err/symmetric_fir_err')
### Starting HDL Check.
...
### HDL Check Complete with 4 errors, warnings and messages.

output =

1x4 struct array with fields:
    path
    type
```

```
message
level

output(1)

ans =

    path: 'sfir_fixed_err/symmetric_fir_err/Product'
    type: 'block'
message: 'Unhandled mixed double and non-double datatypes at ports of block'
level: 'Error'
```

**See Also**      `makehdl`

# hdllib

---

**Purpose** Create Simulink library of blocks that support HDL code generation

**Syntax** `hdllib`

**Description** `hdllib` creates a library of blocks that are supported for HDL code generation. The library is named `hdl_supported.mdl`. After the library is generated, you must save it to a directory of your choice.

`hdllib` loads many Simulink libraries during the creation of the `hdl_supported` library. (This will cause a license checkout.) When `hdllib` completes generation of the library, it does not unload Simulink libraries.

The `hdl_supported` library affords quick access to all supported blocks. By constructing models using blocks from this library, you can ensure block-level compatibility of your model with Simulink HDL Coder.

The set of supported blocks will change in future releases of Simulink HDL Coder. To keep the `hdl_supported.mdl` current, The MathWorks recommends that you rebuild the library and table each time you install a new release.

**Purpose** Generate forEach calls for insertion into code generation control files

**Syntax**

```
hdlnewforeach
hdlnewforeach('blockpath')
hdlnewforeach({'blockpath1','blockpath2',...})
[cmd, impl] = hdlnewforeach
[cmd, impl] = hdlnewforeach('blockpath')
[cmd, impl] = hdlnewforeach({'blockpath1','blockpath2',...})
[cmd, impl, parms] = hdlnewforeach
[cmd, impl, parms] = hdlnewforeach('blockpath')
[cmd, impl, parms] = hdlnewforeach({'blockpath1','blockpath2',
...})
```

**Description** Simulink HDL Coder provides the hdlnewforeach utility to help you construct forEach calls for use in code generation control files. Given a selection of one or more blocks from your model, hdlnewforeach returns the following for each selected block, as string data in the MATLAB workspace:

- A forEach call coded with the correct modelscope, blocktype, and default implementation arguments for the block
- (Optional) A cell array of cell arrays of strings enumerating the available implementations for the block, in package.class form
- (Optional) A cell array of cell arrays of strings enumerating the names of implementation parameters (if any) corresponding to the block implementations. hdlnewforeach does not list data types and other details of block implementation parameters. See “Block Implementation Parameters” on page 5-47 for that information.

hdlnewforeach returns a forEach call for each selected block in the model. Each call is returned as a string.

hdlnewforeach('blockpath') returns a forEach call for a specified block in the model. The call is returned as a string.

The 'blockpath' argument is a string specifying the full Simulink path to the desired block.

# hdlnewforeach

---

`hdlnewforeach({'blockpath1','blockpath2',...})` returns a `forEach` call for each specified block in the model. Each call is returned as a string.

The `{'blockpath1','blockpath2',...}` argument is a cell array of strings, each of which specifies the full Simulink path to a desired block.

`[cmd, impl] = hdlnewforeach` returns a `forEach` call for each selected block in the model to the string variable `cmd`. In addition, the call returns a cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.

`[cmd, impl] = hdlnewforeach('blockpath')` returns a `forEach` call for a specified block in the model to the string variable `cmd`. In addition, the call returns a cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.

The `'blockpath'` argument is a string specifying the full Simulink path to the desired block.

`[cmd, impl] = hdlnewforeach({'blockpath1','blockpath2',...})` returns a `forEach` call for each specified block in the model to the string variable `cmd`. In addition, the call returns a cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.

The `{'blockpath1','blockpath2',...}` argument is a cell array of strings, each of which specifies the full Simulink path to a desired block.

`[cmd, impl, parms] = hdlnewforeach` returns a `forEach` call for each selected block in the model to the string variable `cmd`. In addition, the call returns:

- A cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.
- A cell array of cell arrays of strings (`parms`) enumerating the available implementation parameters corresponding to each implementation.

`[cmd, impl, parms] = hdlnewforeach('blockpath')` returns a `forEach` call for a specified block in the model to the string variable `cmd`. In addition, the call returns:

- A cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.
- A cell array of cell arrays of strings (`parms`) enumerating the available implementation parameters corresponding to each implementation.

The `'blockpath'` argument is a string specifying the full Simulink path to the desired block.

`[cmd, impl, parms] = hdlnewforeach({'blockpath1', 'blockpath2', ...})` returns a `forEach` call for each specified block in the model to the string variable `cmd`. In addition, the call returns:

- A cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.
- A cell array of cell arrays of strings (`parms`) enumerating the available implementation parameters corresponding to each implementation.

The `{'blockpath1', 'blockpath2', ...}` argument is a cell array of strings, each of which specifies the full Simulink path to a desired block.

## Usage Notes

Before invoking `hdlnewforeach`, you must run `checkhdl` or `makehdl` to build in-memory information about the model. If you do not run `checkhdl` or `makehdl`, `hdlnewforeach` will display an error message indicating that you should run `checkhdl` or `makehdl`.

`hdlnewforeach` returns an empty string for blocks that do not have an HDL implementation. `hdlnewforeach` also returns an empty string for subsystems, which are a special case. Subsystems do not have a default implementation class, but special-purpose subsystems implementations

# hdlnewforeach

---

are provided (see Chapter 8, “Interfacing Subsystems and Models to HDL Code”).

After invoking `hdlnewforeach`, you will generally want to insert the `forEach` calls returned by the function into a control file, and use the implementation and parameter information returned to specify a nondefault block implementation. See “Generating Selection/Action Statements with the `hdlnewforeach` Function” on page 5-25 for a worked example.

## Examples

The following example generates `forEach` commands for two explicitly specified blocks.

```
hdlnewforeach({'sfir_fixed/symmetric_fir/Add4',...
'sfir_fixed/symmetric_fir/Product2'})

ans =

c.forEach('sfir_fixed/symmetric_fir/Add4',...
'built-in/Sum', {},...
'hdldefaults.SumLinearHDLEmission', {});

c.forEach('sfir_fixed/symmetric_fir/Product2',...
'built-in/Product', {},...
'hdldefaults.ProductLinearHDLEmission', {});
```

The following example generates a `forEach` command for an explicitly specified `Sum` block. The implementation and parameters information returned is listed after the `forEach` command.

```
[cmd,impl, parms] = hdlnewforeach('sfir_fixed/symmetric_fir/Add4')

cmd =

c.forEach('sfir_fixed/symmetric_fir/Add4',...
'built-in/Sum', {},...
'hdldefaults.SumLinearHDLEmission', {});
```



```
impl =  
  
    {3x1 cell}  
  
parms =  
  
    {1x1 cell}    {1x1 cell}    {1x1 cell}  
>> impl{1}  
  
ans =  
  
    'hdldefaults.SumTreeHDL Emission'  
    'hdldefaults.SumLinearHDL Emission'  
    'hdldefaults.SumCascadeHDL Emission'  
>> parms{1:3}  
  
ans =  
  
    'OutputPipeline'  
  
ans =  
  
    'OutputPipeline'  
  
ans =  
  
    'OutputPipeline'
```

# hdlsetup

---

<b>Purpose</b>	Set Simulink model parameters for HDL code generation
<b>Syntax</b>	<code>hdlsetup</code> <code>hdlsetup('model')</code>
<b>Description</b>	<p><code>hdlsetup</code> changes the parameters of the current Simulink model (bdroot) to values that are commonly used for HDL code generation.</p> <p><code>hdlsetup('model')</code> changes the parameters of the Simulink model specified by the 'model' argument to values that are commonly used for HDL code generation.</p> <p>A model should be open in Simulink before you invoke the <code>hdlsetup</code> command.</p> <p>The <code>hdlsetup</code> command uses the Simulink <code>set_param</code> function to set up models for HDL code generation quickly and consistently. The model parameters settings provided by <code>hdlsetup</code> are intended as useful defaults, but they may not be appropriate for all your applications.</p> <p>To view the complete set of model parameters affected by <code>hdlsetup</code>, view <code>hdlsetup.m</code> in the MATLAB editor.</p> <p>See the “Model Parameters” table in the “Model and Block Parameters” section of the Simulink documentation for a summary of user-settable model parameters.</p>

<b>Purpose</b>	Generate HDL RTL code from Simulink model or subsystem
<b>Syntax</b>	<pre>makehdl() makehdl(bdroot) makehdl('modelName') makehdl('modelName/subsys') makehdl(gcb) makehdl('PropertyName', PropertyValue,...) makehdl(bdroot, 'PropertyName', PropertyValue,...) makehdl('modelName', 'PropertyName', PropertyValue,...) makehdl('modelName/subsys', 'PropertyName', PropertyValue,...) makehdl(gcb, 'PropertyName', PropertyValue,...)</pre>
<b>Description</b>	<p>makehdl generates HDL RTL code (VHDL or Verilog) from a Simulink model or subsystem. We will refer to a model or subsystem from which code is generated as the <i>device under test (DUT)</i>.</p> <p>makehdl() generates HDL code from the current Simulink model (by default), using default values for all properties.</p> <p>makehdl(bdroot) generates HDL code from the current Simulink model, using default values for all properties.</p> <p>makehdl('modelName') generates HDL code from the Simulink model explicitly specified by 'modelName', using default values for all properties.</p> <p>makehdl('modelName/subsys') generates HDL code from a subsystem within the Simulink model specified by 'modelName', using default values for all properties.</p> <p>'subsys' specifies the name of the subsystem. In the current release, this must be a subsystem at the top (root) level of the current Simulink model; it cannot be a subsystem nested at a lower level of the model hierarchy.</p> <p>makehdl(gcb) generates HDL code from the currently selected subsystem within the current Simulink model, using default values for all properties.</p>

`makehdl('PropertyName', PropertyValue, ...)` generates HDL code from the current Simulink model (by default), explicitly specifying one or more code generation options as property/value pairs.

`makehdl(bdroot, 'PropertyName', PropertyValue, ...)` generates HDL code from the current Simulink model, explicitly specifying one or more code generation options as property/value pairs.

`makehdl('modelName', 'PropertyName', PropertyValue, ...)` generates HDL code from the Simulink model explicitly specified by 'modelName', explicitly specifying one or more code generation options as property/value pairs.

`makehdl('modelName/subsys', 'PropertyName', PropertyValue, ...)` generates HDL code from a subsystem within the Simulink model specified by 'modelName', explicitly specifying one or more code generation options as property/value pairs.

'subsys' specifies the name of the subsystem. In the current release, this must be a subsystem at the top (root) level of the current Simulink model; it cannot be a subsystem nested at a lower level of the model hierarchy.

`makehdl(gcf, 'PropertyName', PropertyValue, ...)` generates HDL code from the currently selected subsystem within the current Simulink model, explicitly specifying one or more code generation options as property/value pairs.

Property/value pairs are passed in the form

```
'PropertyName', PropertyValue
```

These property settings determine characteristics of the generated code, such as HDL element naming and whether certain optimizations are applied. The next section, “HDL Code Generation Defaults” on page 14-15, summarizes the default actions of the code generator.

For detailed descriptions of each property and its effect on generated code, see Chapter 13, “Properties — Alphabetical List” and Chapter 12, “Properties — By Category”.

## HDL Code Generation Defaults

This section summarizes the default actions of the code generator. Most defaults can be overridden by passing in appropriate property/value settings to `makehdl`. Chapter 13, “Properties — Alphabetical List” describes all `makehdl` properties in detail.

### Target Language, File Packaging and Naming

- The `TargetLanguage` property determines whether VHDL or Verilog code is generated. The default is VHDL.
- `makehdl` writes generated files to `hdlsrc`, a subdirectory of the current working directory. This directory is called the *target directory*. `makehdl` creates a target directory if it does not already exist.
- `makehdl` generates separate HDL source files for the DUT and each subsystem within it. In addition, `makehdl` generates script files for HDL simulation and synthesis tools. File names derive from the Simulink names of the DUT. File names are assigned by Simulink HDL Coder and are not user-assignable. The following table summarizes file-naming conventions.

<b>File</b>	<b>Name</b>
Verilog source code	<code>system.v</code> , where <i>system</i> is the name of the DUT.
VHDL source code	<code>system.vhd</code> , where <i>system</i> is the name of the DUT.

<b>File</b>	<b>Name</b>
Timing controller code	Timing_Controller.vhd (VHDL) or Timing_Controller.v (Verilog). This file contains a module defining timing signals (clock, reset, external clock enable inputs and clock enable output) in a separate entity or module. Timing controller code is generated if required by the design; a purely combinatorial model does not generate timing controller code.
ModelSim compilation script	<i>system_compile.do</i> , where <i>system</i> is the name of the DUT.
Synplify synthesis script	<i>system_synplify.tcl</i> , where <i>system</i> is the name of the DUT.
VHDL package file	<i>system_pkg.vhd</i> , where <i>system</i> is the name of the DUT. A package file is generated only if the design requires a VHDL package.
Mapping file	<i>system_map.txt</i> , where <i>system</i> is the name of the DUT. This report file maps generated entities (or modules) to the Simulink subsystems that generated them. See “Code Tracing Using the Mapping File” on page 7-6.

## Entities, Ports, and Signals

- Unique names are assigned to generated VHDL entities or Verilog modules. Entity or module names are derived from the

names of the DUT. Name conflicts are resolved by the use of a postfix string.

- HDL port names are assigned according to the following conventions:

<b>HDL Port</b>	<b>Name</b>
Input	Same as corresponding port name on the DUT (name conflicts resolved according to rules of the target language)
Output	Same as corresponding port name on the DUT (name conflicts resolved according to rules of the target language)
Clock input	clk
Clock enable input	clk_enable
Clock enable output	ce_out
Reset input	reset

- HDL port directions and data types
  - Port direction: IN or OUT, corresponding to the port on the DUT.
  - Clock, clock enable, and reset port data types: VHDL type `STD_LOGIC_VECTOR` or Verilog type `wire`.
  - Input and output port data types: VHDL type `STD_LOGIC_VECTOR` or Verilog type `wire`. Port widths are determined by Simulink.
- HDL signal names and data types:
  - HDL signals generated from named Simulink signals retain their signal names.

- For unnamed Simulink signals, HDL signal names are derived from the concatenated names of the block and port connected to the signal in the DUT: *blockname\_portname*. Conflicting names are made unique according to VHDL or Verilog rules.
- Signal data types are determined by the data type of the corresponding Simulink signal. Each signal declaration is annotated with a comment indicating the Simulink data type.

## General HDL Code Settings

- VHDL-specific defaults:
  - Generated VHDL files include both entity and architecture code.
  - VHDL configurations are placed in any file that instantiates a component.
  - VHDL code checks for rising edges via the logic `IF clock'event AND clock='1' THEN...`, when operating on registers.
  - When creating labels for VHDL GENERATE statements, makehdl appends `_gen` to section and block names. makehdl names output assignment block labels with the string `outputgen`.
- A type-safe representation is used for concatenated zeros: `'0' & '0'...`
- Generated code for registers uses asynchronous reset logic with an active-high (1) reset level.
- The postfix string `_process` is appended to process names.
- For Microsoft Windows, carriage return/linefeed (CRLF) character sequences are never emitted in generated code.



## Code Optimizations

- In general, generated HDL code produces results that are bit-true and cycle-accurate with respect to the original Simulink model (that is, the HDL code exactly reproduces simulation results from the Simulink model).

However, some block implementations generate code that includes certain block-specific performance and area optimizations. These optimizations can produce numeric results or timing differences that differ from those produced by the original Simulink model (see Chapter 6, “Generating Bit-True Cycle-Accurate Models”).

## Examples

- The following call to `makehdl` generates Verilog code for the subsystem `symmetric_fir` within the model `sfir_fixed`.

```
makehdl('sfir_fixed/symmetric_fir','TargetLanguage','Verilog')
```

- The following call to `makehdl` generates VHDL code for the current model. Code is generated into the target directory `hdlsrc`, with all code generation options set to default values.

```
makehdl(bdroot)
```

- The following call to `makehdl` directs the HDL compatibility checker (see `checkhdl`) to check the subsystem `symmetric_fir` within the model `sfir_fixed` before code generation starts. If no compatibility errors are encountered, `makehdl` generates VHDL code for the subsystem `symmetric_fir`. Code is generated into the target directory `hdlsrc`, with all code generation options set to default values.

```
makehdl('sfir_fixed/symmetric_fir','CheckHDL','on')
```

## See Also

`makehdltb`, `checkhdl`

# makehdltb

---

**Purpose** Generate HDL test bench from Simulink model

**Syntax**

```
makehdltb('modelName/subsys')  
makehdltb('modelName/subsys', 'PropertyName', PropertyValue,  
...)
```

**Description** `makehdltb('modelName/subsys')` generates an HDL test bench from the specified subsystem within a Simulink model, using default values for all properties. The *modelName/subsys* argument gives the Simulink path to the subsystem under test. This subsystem must be at the top (root) level of the current Simulink model. The generated test bench is designed to interface to and validate HDL code generated from *subsys* (or from a subsystem with a functionally identical public interface).

A typical practice is to generate HDL code for a subsystem, followed immediately by generation of a test bench to validate the same subsystem (see “Examples” on page 14-23).

---

**Note** If `makehdl` has not previously executed successfully within the current MATLAB session, `makehdltb` generates model code before generating the test bench code.

Test bench code and model code must both be generated in the same target language. If the target language specified for `makehdltb` differs from the target language specified for the previous `makehdl` execution, `makehdltb` will regenerate model code in the same language specified for the test bench.

Properties passed in to `makehdl` persist after `makehdl` executes, and (unless explicitly overridden) will be passed in to subsequent `makehdltb` calls during the same MATLAB session.

---

`makehdltb('modelName/subsys', 'PropertyName', PropertyValue, ...)` generates an HDL test bench from the specified

subsystem within a Simulink model, explicitly specifying one or more code generation options as property/value pairs.

Property/value pairs are passed in the form

```
'PropertyName', PropertyValue
```

These property settings determine characteristics of the test bench code. Many of these properties are identical to those for `makehdl`, while others are specific to test bench generation (for example, options for generation of test bench stimuli). The next section, “Defaults for Test Bench Code Generation” on page 14-21, summarizes the defaults that are specific to generated test bench code.

For detailed descriptions of each property and its effect on generated code, see Chapter 13, “Properties — Alphabetical List” and Chapter 12, “Properties — By Category”.

## Generating Stimulus and Output Data

`makehdltb` generates test data from Simulink signals connected to inputs of the subsystem under test. Sample values for each stimulus signal are computed and stored for each time step of the simulation. The signal data is represented as arrays in the generated test bench code.

To help you validate generated HDL code, `makehdltb` also generates output data from Simulink signals connected to outputs of the subsystem under test. Like input data, sample values for each output signal are computed and stored for each time step of the simulation. The signal data is represented as arrays in the generated test bench code.

The Simulink total simulation time (set by the model’s **Stop Time** parameter) determines the size of the stimulus and output data arrays. Computation of sample values can be time-consuming. Consider speeding up generation of signal data by entering a shorter **Stop Time**.

## Defaults for Test Bench Code Generation

This section describes defaults that apply specifically to generation of test bench code. `makehdltb` has many properties and defaults in

common with makehdl. See “HDL Code Generation Defaults” on page 14-15 for a summary of these common properties and defaults.

## File Packaging and Naming

makehdltb generates an HDL source file containing test bench code and arrays of stimulus and output data. In addition, makehdltb generates script files that let you execute a ModelSim simulation of the test bench and the HDL entity under test. Generated test bench file names (like makehdl generated file names) are based on the name of the DUT. The following table summarizes the default test bench file-naming conventions.

<b>File</b>	<b>Name</b>
Verilog test bench	<i>system_tb.v</i> , where <i>system</i> is the name of the system under test
VHDL test bench	<i>system_tb.vhd</i> , where <i>system</i> is the name of the system under test
ModelSim compilation script	<i>system_tb_compile.do</i> , where <i>system</i> is the name of the DUT
ModelSim simulation script	<i>system_tb_sim.do</i> , where <i>system</i> is the name of the DUT

## Other Test Bench Settings

- The test bench forces clock, clock enable, and reset input signals.
- The test bench forces clock enable and reset input to active high (1).
- The clock input signal is driven high (1) for 5 nanoseconds and low (0) for 5 nanoseconds.
- The test bench forces reset signals.

- The test bench applies a hold time of 2 nanoseconds to reset and data input signals.

## Examples

In the following example, makehdl generates VHDL code for the subsystem `symmetric_fir`. After Simulink HDL Coder indicates successful completion of code generation, makehdltb generates a VHDL test bench for the same subsystem.

```
makehdl('sfir_fixed/symmetric_fir')
### Applying HDL Code Generation Control Statements

### Begin VHDL Code Generation
### Working on sfir_fixed/symmetric_fir ashdlsrc\symmetric_fir.vhd
### HDL Code Generation Complete.
makehdltb('sfir_fixed/symmetric_fir')
### Begin TestBench Generation
### Generating Test bench:hdlsrc\symmetric_fir_tb.vhd
### Please wait ...

### HDL TestBench Generation Complete.
```

## See Also

makehdl



# Examples

---

Use this list to find examples in the documentation.

## **Generating HDL Code Using MATLAB Commands**

- “Creating a Directory and Local Model File” on page 2-6
- “Initializing Model Parameters with hdlsetup” on page 2-7
- “Generating a VHDL Entity from a Subsystem” on page 2-9
- “Generating VHDL Test Bench Code” on page 2-11
- “Verifying Generated Code” on page 2-12
- “Creating the Model and Configuring General Model Settings” on page 10-10

## **Generating HDL Code in the Simulink Environment**

- “Creating a Directory and Local Model File” on page 2-18
- “Viewing Simulink HDL Coder Options in the Configuration Parameters Dialog Box” on page 2-19
- “Initializing Model Parameters With hdlsetup” on page 2-24
- “Selecting and Checking a Subsystem for HDL Compatibility” on page 2-26
- “Generating VHDL Code” on page 2-27
- “Generating VHDL Test Bench Code” on page 2-29
- “Verifying Generated Code” on page 2-31

## **Verifying Generated HDL Code in an HDL Simulator**

- “Simulating and Verifying Generated HDL Code” on page 2-32



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